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Nonlinear control for a DC–DC converter with dual active bridges in a DC microgrid

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ABSTRACT

This work presents a new control strategy for a DC–DC converter with dual active bridges used to interconnect two feeders in a DC microgrid. The proposed control strategy allows regulating the output voltage of the converter while maintaining the mean primary and secondary current value of the high-frequency transformer at zero, in order to avoid magnetic saturation. The controller is designed using the nonlinear control strategy based on feedback linearization, which is based on the converter generalized space-state averaged model. The performance of the proposed controller is validated via simulation and experimental results.

1. Introduction

The DC–DC converter with dual active bridges (DAB), first presented in [1], is a topology comprising two three-phase [1] or single-phase [2] active bridges, interconnected by means of a high-frequency transformer (HFT).

In the last decades, this topology has gained academic and industrial importance due to its ability to allow bidirectional power flow, galvanic isolation, and the possibility to increase efficiency by means of soft switching techniques [3]. These features make it attractive for electric mobility applications [2,4], energy storage systems (ESS) [5], solid-state transformers (SST), [6], and even for the new electrical network schemes, such as DC microgrids (MG) [7,8].

Therefore, in light of the growing relevance that this topology has acquired, there are research works in the literature that propose diverse modeling techniques for obtaining the mathematical model of the converter, given that this is crucial for analyzing their dynamic behavior and for designing control strategies. In [9] the reduced order model of the converter is obtained, which only considers the dynamics of the input and output voltage and disregards the dynamics of the primary and secondary currents on the HFT. On the other hand, in [10], the classical state-space averaging (SSA) model of the converter is obtained, which considers the dynamics of the output voltage and the mean value of the primary current of the HFT. Meanwhile, in [11,12], the generalized state-space averaging (GSSA) modeling strategy is employed in order to obtain a model that describes the dynamics of the output voltage and from the fundamental component of the primary current of the HFT.

In addition to mathematical modeling, there are also works in the literature where control strategies are designed for DC–DC DAB converters. Some of them are based on power control, such as [13], which proposes a direct power control strategy using a classical controller, which is designed based on the reduced order model of the converter.

On the other hand, there are works that propose the design of control strategies to regulate the output voltage of the converter by using linear control tools [11], as well as nonlinear ones such as passivity-based control [2,14], input–output feedback linearization (IO-FL) [15], or sliding mode control (SMC) [16,17], among others.

Control strategies based on linear tools are easy to design and simple to implement. However, given that they are designed based on the linearized version of the non-linear model of the DC–DC DAB converter, they are only valid in proximity to the considered operation point. Therefore, they can have performance and stability issues when large load changes, reference changes, and parametric variations occur; whereas control strategies designed by means of nonlinear tools have a good performance and guarantee the system's stability throughout the range of operation of the converter [18].

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Even though the aforementioned control strategies allow regulating the output voltage of the converter according to the reference value, they consider that the mean value from the primary and secondary current of the HFT is zero. This consideration is only valid under ideal operating conditions, since, under real conditions such as a difference in the conduction resistance of the power devices or different delays in the commutation signals, an average value can occur in the primary and secondary current of the HFT that increases the converter's losses and may even entail the magnetic saturation of the HFT [19].

To solve this issue, some works propose the addition of a capacitor in series with the HFT in order to block the DC component in the primary and secondary currents of the HFT [20], although this solution increases the volume and cost of the system.

Another approach is based on developing commutation techniques in order to eliminate the mean value in the primary and secondary currents of the HFT [21]. A third approach available in the literature is based on developing control strategies whose objective is to maintain the mean value of these currents at zero, as is the case of [19,22], where linear control techniques are employed. In this way, easy-to-implement controllers are obtained, but their design is based in the averaged model of the converter, which means that they do not take into account the AC component dynamics from the primary and secondary currents of the HFT. Also, they are only valid in the proximity of the considered operation point, given that, within their design, the linearized version of the nonlinear model of the converter is used. Therefore, its performance can decrease and even become unstable under disturbances such as large load variations or reference changes.

This work proposes a new control strategy for a DC–DC DAB converter used to interconnect two feeders in a DC MG operating at different voltage levels. Unlike the existing proposals, in this work, a nonlinear control strategy is designed by means of IO-FL in order to regulate the output voltage of the converter according to a required reference value while maintaining the mean value from the primary and secondary currents of the HFT at zero, with the purpose of preventing magnetic saturation and reducing the losses of the system.

Since the DC–DC DAB converter has two DC stages and one AC stage, in order to obtain its mathematical model, this work utilizes the GSSA modeling technique with the purpose of including the dynamic behavior of the fundamental AC component from the primary current of the HFT, given that it is considered to be relevant in controller design. On the other hand, due to the fact that the voltage controller is designed to be ten times slower than the controller for the mean value from the primary and secondary current of the HFT, the GSSA converter model may be separated in two parts, so that easy-to-implement controllers are obtained which also ensure stability and an excellent dynamic performance against reference changes, large load variations, and even the connection of destabilizing loads, as is the case of constant power loads (CPL).

This work is organized as follows: Section 2 describes the converter model; Section 3 presents the proposed control strategy; Section 4 shows the obtained results; and, finally, Section 5 provides the conclusions and the final discussion.

2. Mathematical modeling of the converter

The considered system is shown in Fig. 1(a), and it comprises two single-phase active bridges interconnected by an HFT. The commutation signal u_1 for active bridge 1 is a PWM signal, whereas the commutation signal u_2 for active bridge 2 is a square signal modulated by phase shift, as shown in Fig. 1(b). Whereas, i_{in} is the input current, i_{P_1} is the current of active bridge 1, v_i is the input voltage (considered to be constant), C_i is the input capacitor, v_p and v_s correspond to the primary and secondary voltages of the HFT, i_{t_1} and i_{t_2} correspond to the primary and secondary currents of the HFT, n is the turns ratio of the HFT, i_{P_2} the current of the active bridge 2, i_0 is the output current, v_0 is the output voltage and C_0 is the output capacitor.

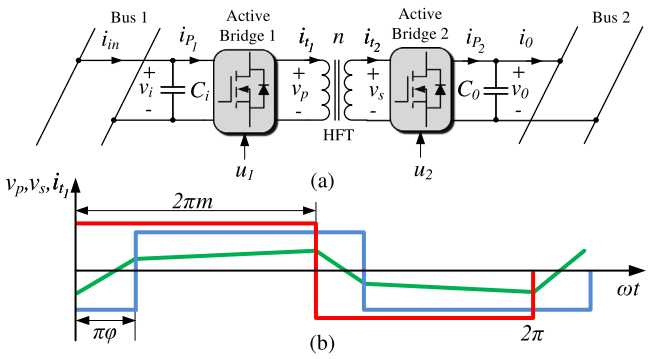

Fig. 1. DC–DC DAB converter. (a) Topological scheme, (b) primary voltage v_p (red), secondary voltage v_s (blue), and current on the primary winding of the HFT (green).

By means of the duty cycle m of the v_p of the HFT, the mean value of the primary and secondary current of the HFT is maintained at zero, while the phase shift φ applied to the secondary voltage of the HFT allows regulating the output voltage of the converter according to the reference value.

The expression for the power transferred when the converter is in steady state ($m = 0.5$) is given by,

$$P_0 = \frac{n v_i v_0}{2 f_s L_t}\varphi(1 - |\varphi|) = i_0 v_0, \tag{1}$$

where f_s the commutation frequency, and L_t is the leakage inductance of the HFT. Meanwhile, the phase shift is between $0 \leq \varphi \leq 1$, given that, without losing generality, this work considers the power flow to be from active bridge 1 towards active bridge 2.

To design a control strategy that allows fulfilling the required objectives, a mathematical model must be obtained which describes the dynamic behavior of the converter.

Given that the DC–DC DAB converter has two DC stages (input and output) and an AC one (made up by the HFT), the GSSA modeling strategy is employed to obtain its mathematical model, since this method allows including the dynamic behavior of the AC variables' relevant harmonics [12]. Fundamentals of the GSSA modeling strategy used in this work are described in Appendix A.

In order to obtain the GSSA model of the DC–DC DAB converter, only the mean value ($k = 0$) of the output voltage is considered since it is a DC variable, while, as for the primary current of the HFT, its mean value ($k = 0$) and its AC fundamental component ($k = 1$) are considered. Thus, the GSSA model is as follows [7]:

$$C_0\dot{x}_1 = 2n\left(\mu_1 x_2 + \mu_2 x_3\right) - i_0, \tag{2}$$

$$L_t\dot{x}_2 = \omega L_t x_3 - R_t x_2 + \alpha_1 v_i - n\mu_1 x_1, \tag{3}$$

$$L_t\dot{x}_3 = -\omega L_t x_2 - R_t x_3 + \alpha_2 v_i - n\mu_2 x_1, \tag{4}$$

$$L_t\dot{x}_4 = -R_t x_4 + \alpha_0 v_i - \mu_0 x_1, \tag{5}$$

where R_t is the equivalent resistance of the HFT, $\omega = 2\pi f_s$, while,

$$\begin{aligned} &x_1 = \langle v_0\rangle_0,\ x_2 = \langle i_{t_1}\rangle_{1R},\ x_3 = \langle i_{t_1}\rangle_{1I},\ x_4 = \langle i_{t_1}\rangle_0,\ i_0 = \langle i_0\rangle_0,\\ &v_i = \langle v_i\rangle_0,\ \alpha_0 = \langle u_1\rangle_0,\ \alpha_1 = \langle u_1\rangle_{1R},\ \alpha_2 = \langle u_1\rangle_{1I},\ \mu_0 = \langle u_2\rangle_0 = 0,\\ &\mu_1 = \langle u_2\rangle_{1R} = -\frac{2}{\pi}\sin(\pi\varphi),\ \mu_2 = \langle u_2\rangle_{1I} = -\frac{2}{\pi}\cos(\pi\varphi), \end{aligned} \tag{6}$$

whereas the complex number $\langle x\rangle_k$ represents the kth coefficient of the Fourier series of the state and input variables, and is defined by the sliding average for a switching period T_s, and the "0" subindex denotes the DC component and subindex "1R" and "1I" represent the real and imaginary part of the fundamental component [7].

Since this work designs the voltage controller to have a settling time slower than the control loop for the mean primary and secondary the HFT current value, the model given by (2)–(5) may be separated,

thus obtaining a model that describes the dynamics of the component ($k = 0$) for the output voltage and the dynamics of the fundamental component ($k = 1$) corresponding to the primary current of the HFT. This design allows to represent the slow dynamics of the system by grouping the expressions (2)–(4), which results as shown in (7)–(9) after considering the commutation signal u_1 to have a 50% duty cycle. Therefore, $\alpha_0 = \alpha_1 = 0$ and $\alpha_2 = -2/\pi$, and the model for the slow dynamics results as follows:

$$C_0\dot{x}_1 = 2n\left(\mu_1 x_2 + \mu_2 x_3\right) - i_0, \tag{7}$$

$$L_t\dot{x}_2 = \omega L_t x_3 - R_t x_2 - n\mu_1 x_1, \tag{8}$$

$$L_t\dot{x}_3 = -\omega L_t x_2 - R_t x_3 - n\mu_2 x_1 - \frac{2}{\pi}v_i. \tag{9}$$

On the other hand, the fast dynamics of the system, which describe the component ($k = 0$) from the primary current of the HFT, are obtained after considering that commutation signal u_1 did not reach the equilibrium point corresponding to a 50% duty cycle. Thus,

$$L_t\dot{x}_4 = -R_t x_4 + d v_i, \tag{10}$$

where $d = \alpha_0 = 2m - 1$, and m is the duty cycle of u_1.

Next, expressions (7)–(10) are evaluated at the equilibrium point. To this effect, R_t is neglected, since it is generally a small value, thus obtaining the following:

$$m^e = \frac{1}{2},\quad x_2^e = \frac{1}{\pi\omega L_t}\left(-n\pi v_0^d \mu_2^e - 2v_i\right), \tag{11}$$

where, m^e, μ_1^e, and μ_2^e are the equilibrium points of the control variables, and v_0^d is the desired output voltage. On the other hand, the phase shift equilibrium point is obtained through (1):

$$\varphi^e = \frac{1}{2}\left(1 - \sqrt{1 - \frac{8 f_s L_t i_0^e}{n v_i}}\right), \tag{12}$$

where i_0^e is the output current of the converter at the equilibrium point.

3. Control strategy

This section presents the control strategy proposed to fulfill the control objectives with the established design requirements. In order to regulate the output voltage according to a required reference value and to maintain the mean value from the primary and secondary current of the HFT at zero, a control strategy based on IO-FL is designed in this work.

This strategy turns the nonlinear model of the DC–DC DAB converter, which is given by (7)–(10), into a linear equivalent, which is also controllable from upon the basis of a coordinate change and nonlinear feedback. This cancels the nonlinearities of the (7)–(10) system, thus allowing to design a linear controller in order to fulfill the established performance objectives [23].

To design an IO-FL control strategy, the (7)–(10) system must first be written as a control-affine system [18],

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}) + \mathbf{g}(\mathbf{x})\mathbf{u}, \tag{13}$$

$$\mathbf{y} = \mathbf{h}(\mathbf{x}), \tag{14}$$

where,

$$\mathbf{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix},\ \mathbf{f}(\mathbf{x}) = \begin{bmatrix} -\frac{1}{C_0}i_0 \\ -\frac{R_t}{L_t}x_2 + \omega x_3 \\ -\omega x_2 - \frac{R_t}{L_t}x_3 - \frac{2}{\pi L_t}v_i \\ -\frac{R_t}{L_t}x_4 - \frac{1}{L_t}v_i \end{bmatrix},$$
$$\mathbf{g}(\mathbf{x}) = \begin{bmatrix} \frac{2n}{C_0}x_2 & \frac{2n}{C_0}x_3 & 0 \\ -\frac{n}{L_t}x_1 & 0 & 0 \\ 0 & -\frac{n}{L_t}x_1 & 0 \\ 0 & 0 & \frac{2}{L_t}v_i \end{bmatrix},\ \mathbf{u} = \begin{bmatrix} \mu_1 \\ \mu_2 \\ m \end{bmatrix}. \tag{15}$$

Given that the output voltage of the converter is indirectly controlled (see Fig. 2), whereas the average value of the primary current of the HFT is directly controlled (see Fig. 2), the selected output vector is the following,

$$\mathbf{y} = \begin{bmatrix} y_1 & y_2 & y_3 \end{bmatrix}^T = \begin{bmatrix} x_2 & x_3 & x_4 \end{bmatrix}^T. \tag{16}$$

By deriving (16) with respect to the time until the inputs to explicitly appear, the following is obtained:

$$\begin{bmatrix} \dot{y}_1 & \dot{y}_2 & \dot{y}_3 \end{bmatrix}^T = \begin{bmatrix} \dot{x}_2 & \dot{x}_3 & \dot{x}_4 \end{bmatrix}^T = \mathbf{A}(\mathbf{x}) + \mathbf{E}(\mathbf{x})\mathbf{u}, \tag{17}$$

where,

$$\mathbf{A}(\mathbf{x}) = \begin{bmatrix} -\frac{R_t}{L_t}x_2 + \omega x_3 \\ -\omega x_2 - \frac{R_t}{L_t}x_3 - \frac{2}{\pi L_t}v_i \\ -\frac{R_t}{L_t}x_4 - \frac{2}{\pi L_t}v_i \end{bmatrix},$$
$$\mathbf{E}(\mathbf{x}) = \begin{bmatrix} -\frac{n}{L_t}x_1 & 0 & 0 \\ 0 & -\frac{n}{L_t}x_1 & 0 \\ 0 & 0 & \frac{2}{L_t}v_i \end{bmatrix}. \tag{18}$$

Matrix $\mathbf{E}(\mathbf{x})$ in (18) is nonsingular, since the input and output voltages are both higher than zero. Therefore, based on (17), it is possible to obtain the control inputs.

Next, an auxiliary control input vector is defined:

$$\begin{bmatrix} \gamma_1 & \gamma_2 & \gamma_3 \end{bmatrix}^T = \begin{bmatrix} \dot{x}_2 & \dot{x}_3 & \dot{x}_4 \end{bmatrix}^T. \tag{19}$$

Finally, after replacing (18) and (19) into (17), the control inputs are as follows:

$$\mu_1 = -\frac{L_t}{n x_1}\left(\gamma_1 + \frac{R_t}{L_t}x_2 - \omega x_3\right), \tag{20}$$

$$\mu_2 = -\frac{L_t}{n x_1}\left(\gamma_2 + \omega x_2 + \frac{R_t}{L_t}x_3 + \frac{2}{\pi L_t}v_i\right), \tag{21}$$

$$m = \frac{1}{2}\left(\frac{L_t}{v_i}\left(\gamma_3 + \frac{R_t}{L_t}x_4\right) + 1\right). \tag{22}$$

Expressions (20) and (21) correspond to the real and imaginary parts of the control variable φ, which represents the phase shift that must be applied between the primary (v_p) and secondary (v_s) voltages of the HFT in order to regulate the output voltage according to the required value. Meanwhile, expression (22) corresponds to the duty cycle used to generate the PWM signal in active bridge 1 (u_1), which allows maintaining the mean value of the primary and secondary currents of the HFT at zero.

3.1. External control loop design

With the purpose of regulating the output voltage, an external control loop is designed, as shown in Fig. 2.

With this aim, the external control loop is considered lower than the internal control loop, i.e. $x_2 = x_2^d$ and $x_3 = x_3^d$. Then, if the control inputs in (7) are replaced by (20) and (21), and both members are multiplied by x_1, the following is obtained:

$$C_0\dot{x}_1^2 = -4R_t\left(\left(x_2^d\right)^2 + \left(x_3^d\right)^2\right) - \frac{8}{\pi}v_i x_3^d - i_0 x_1, \tag{23}$$

By defining,

$$\eta = -4R_t\left(\left(x_2^d\right)^2 + \left(x_3^d\right)^2\right) - \frac{8}{\pi}v_i x_3^d - i_0 x_1. \tag{24}$$

x_3^d can be obtained from:

$$x_3^d = \frac{1}{2}\left(-b \pm \sqrt{b^2 - 4\left(\left(x_2^d\right)^2 + \frac{c}{4R_t}\right)}\right), \tag{25}$$

where $b = \frac{2v_i}{\pi R_t}$, $c = 2i_0 x_1 + \eta$ and η is an auxiliary control input designed as follows,

$$\eta = -k_{p_1}\left(\sigma - \left(v_0^d\right)^2\right) - k_{i_1}\int\left(\sigma - \left(v_0^d\right)^2\right)dt, \tag{26}$$

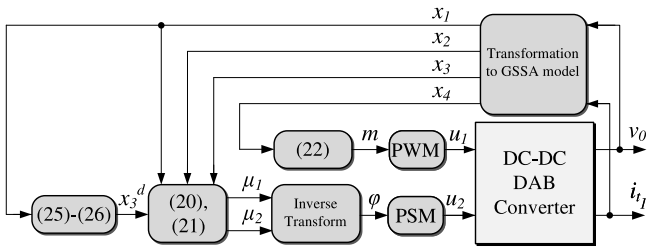

Fig. 2. Proposed control scheme.

where $\sigma = x_1^2$, k_{p_1} is a proportional gain that allows obtaining the desired convergence of the output voltage error to zero, whereas k_{i_1} is an integral gain that is added to eliminate the steady state error in the output voltage when parameter variations and other disturbances not included in the model occur.

3.2. Design of the control parameters for the internal loop

In this section, the auxiliary control inputs given by (19) are designed. To this effect, the errors are defined as $e_2 = x_2 - x_2^d$, $e_3 = x_3 - x_3^d$ and $e_4 = x_4 - x_4^d$, and their dynamics are set as follows:

$$\begin{aligned} \dot{e}_2 + k_{p_2} e_2 &= 0, \\ \dot{e}_3 + k_{p_3} e_3 &= 0, \\ \dot{e}_4 + k_{p_4} e_4 &= 0, \end{aligned} \tag{27}$$

where $x_2^d = x_2^e$, x_3^d is obtained by means of the external control loop described in the previous section, and $x_4^d = 0$, since the objective of the controller for the mean value of the primary and secondary current of the HFT is to maintain both with a zero mean value, to avoid magnetic saturation of the HFT.

By replacing (19) into (27), the following auxiliary control inputs are obtained:

$$\gamma_1 = -k_{p_2}(x_2 - x_2^d), \tag{28}$$

$$\gamma_2 = -k_{p_3}(x_3 - x_3^d), \tag{29}$$

$$\gamma_3 = -k_{p_4}(x_4 - x_4^d) - k_{i_4} \int (x_4 - x_4^d) dt, \tag{30}$$

where k_{p_j} (with $j = 2, 3, 4$) are the proportional gains, whereas k_{i_4} is an integral gain that is added with the purpose of eliminating the steady state error in the mean value of the primary and secondary currents of the HFT. These gains must be adjusted in order to obtain the desired response, and they must also ensure that the poles of (27) are located in the left half-plane.

Finally Fig. 2 shows the proposed control scheme. The GSSA components are extracted by means of low pass filtering processes, which is detailed in Appendix B [24]. Then, the variables (x_1, x_2, and x_3) are used to obtain the control variables (μ_1 and μ_2), which, after an inverse transformation, allow obtaining the phase shift φ that is applied to a phase shift modulation (PSM) block, which generates activation signals for the power transistors for the active bridge 2.

Similarly, the variable x_4 is also obtained through GSSA transformation, which is also used to obtain the control variable m applied to a PWM block in order to generate the activation signals for the active bridge 1.

3.3. Stability analysis for the zero-dynamics

The selected outputs (16) show a relative degree ($r = 3$), whereas the system order is four ($n = 4$). Therefore, there is a zero-dynamics given by (7) whose stability must be verified.

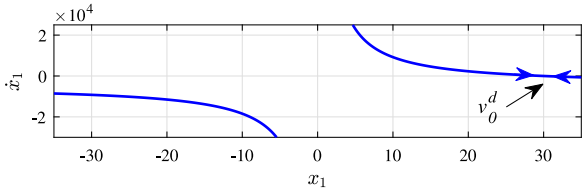

Fig. 3. Phase portrait of the zero-dynamics given by (31).

Table 1
Converter parameters.

v_i	v_0^d	f_s	n	L_t	R_t	C_0
40 V	25 V	20 kHz	1	29 μH	0.1 Ω	940 μF

If the control inputs (20) and (21) are replaced into (7) and it is considered that $x_2 = x_2^d$, $x_3 = x_3^d$, and $i_0 = i_0^e$, the following is obtained:

$$\dot{x}_1 = \frac{2}{C_0 x_1}\left(-R_t\left(\left(x_2^d\right)^2 + \left(x_3^d\right)^2\right) - \frac{2}{\pi} v_i x_3^d\right) - \frac{i_0^e}{C_0}. \tag{31}$$

Expression (31) corresponds to the resulting zero-dynamics. Fig. 3 shows their phase portrait using the parameters in Table 1 and considering the most unfavorable stability case, which occurs when only one CPL is connected to feeder 2 of the system shown in Fig. 1(a). This means that $\left(i_0^e = P_{CPL}/v_0^d\right)$, where $P_{CPL} = 150$ W.

The zero-dynamics given by (31) has a single equilibrium point given by v_0^d, and it is of minimum phase (see Fig. 3). Therefore, the designed controller ensures that the closed-loop system is stable.

4. Results

To validate the performance of the proposed control strategy for the DC–DC DAB converter, simulation and experimental results are shown, which were obtained by means of a prototype built in the Laboratorio de Control Automático (LCA) of the Facultad de Ingeniería *y* Ciencias Agropecuarias of Universidad Nacional de San Luis.

4.1. Simulation results

The simulations of the system were performed using Matlab's SimPowerSystem library. The simulated converter constitutes a realistic model that includes the losses in MOSFET semiconductor devices with an internal resistance $R_d = 40$ mΩ, whereas the simulation was performed with a fixed step size $T = 25$ ns via the ode4 solver (Runge–Kutta).

To perform the simulations, the control scheme in Fig. 2 was used, which was applied to the system shown in Fig. 1(a), connecting a DC voltage source (v_i) to feeder 1 while linear loads and a CPL are connected to feeder 2. The objective of the DC–DC DAB converter is to adapt the voltage levels between both feeders, meanwhile that the controller objective is to regulate the voltage in feeder 2 according to a required reference value, and, at the same time, maintain the mean value of the primary and secondary current from the HFT at zero.

Table 1 shows the parameters of the converter.

The gains of the voltage controller were adjusted in order to obtain a settling time of 2 ms, and their values are $k_{p_1} = 0.66$, $k_{p_2} = 7e4$, $k_{p_3} = 15e4$, and $k_{i_1} = 0.19$. On the other hand, as for the controller that allows maintaining the mean value of the primary and secondary HFT currents at zero, the gains were adjusted in order to obtain a settling time of 0.2 ms, and their resulting values were $k_{p_4} = 1e4$ and $k_{i_4} = 0.001$.

The simulation has a duration of 35 ms and consists of a reference change carried out at $t = 10$ ms, where the reference voltage was modified from 25 to 30 V. Subsequently, at $t = 20$ ms, the linear load was increased from 50 to 100 W. Finally, at $t = 30$ ms, the linear

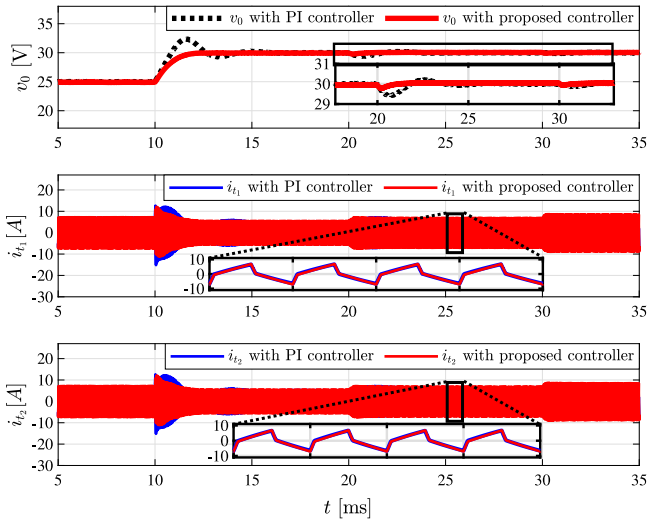

Fig. 4. Converter's response to reference change and load variations. Top: output voltage. Center: primary HFT current. Bottom: secondary HFT current.

load was disconnected and a 150 W CPL was connected. Also, the internal resistance of the MOSFET of active bridge 1 was modified from its nominal value R_d = 40 mΩ to R_d = 60 mΩ to validate the performance of the controller of the mean value of the primary and secondary current of the HFT.

Fig. 4 (top) shows the output voltage of the converter. When the reference changes, at t = 10 ms, the output voltage is controlled to achieve the new reference value after 2 ms without any overshoot or oscillations.

Afterwards, while performing the linear load change in t = 20 ms, a decrease in the output voltage lower than 1% with respect to the reference value is observed, and then it returns to the reference value within the expected settling time with no oscillations.

Finally, when the linear load is disconnected and the CPL is connected at t = 30 ms, the output voltage shows a decrease of approximately 0.5% with respect to the reference value, and it then returns to the reference value within the required settling time. It is observed that, in light of the reference change and the load variations, the output voltage meets the required settling time, and it provides a response with no oscillations or steady state errors. Furthermore, it can be seen that during the disturbances produced during the linear load change and the connection of the CPL, the output voltage shows a small decrease, which, in both cases, does not exceed 1% with respect to the reference value.

On the other hand, Fig. 4 (center and bottom) shows the primary and secondary currents of the HFT. It is observed that, during the whole test, both currents show transients without any excessive overshoot (with the worst case being the reference voltage change). Besides, it is observed that both currents maintain their mean value at zero during steady state operation. The latter may be verified with the detail seen at t = 25 ms, from 0.2 ms in duration, where the waveforms of both currents are found to have zero mean value during steady state.

In addition, Fig. 4 shows the response obtained for the same test but using two PI controllers, one to regulate the output voltage and the other to keep the mean value of the primary and secondary current of the HFT at zero. The gains of both controllers were adjusted to obtain the same settling time as with the proposed controller, resulting in k_{p_v} = 0.06 and k_{i_v} = 75 for the voltage controller, whereas for the current controller results in the following gains k_{p_i} = 0.009 and k_{I_i} = 120. Details about the design of the PI-based controller for the considered system and a comparison with the controller without mean value control of the HFT current can be found in [7].

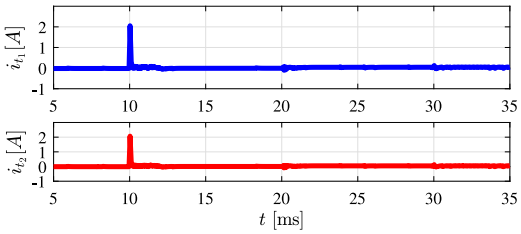

Fig. 5. Mean value of the HFT currents for the proposed controller. Top: Mean value of the primary HFT current. Bottom: Mean value of the secondary HFT current.

In Fig. 4 (top) the output voltage is shown (in dashed lines) for the PI controller. A lower performance is observed with respect to the proposed controller, since a transient response with overshoot and oscillations is obtained. Whereas in Fig. 4 (center and bottom) the primary and secondary current of the HFT are shown respectively (both in blue). It is observed that the currents remain with zero mean value at steady state, although they present a transient response with oscillations and greater overshoot, compared with the proposed controller.

Finally, Fig. 5 shows the mean value of both currents of the HFT for the proposed controller. In steady state, both currents maintain their mean value at zero, with small transients at the moments of reference and load changes, whose overshoot is lower than 2 A in the worst case (reference change).

4.2. Experimental results

In order to validate experimentally the control strategy proposed in this work, a laboratory prototype was used. It is an isolated DC–DC DAB converter, with an HFT that have a unitary turns ratio. The power switches used in the converter are IRFP260 MOSFET's. The parameters of this converter are those listed in Table 1. The control strategy was implemented in a Texas Instruments TMS320F28377D DSC using the same gains as those used in the simulation. Fig. 7 shows a picture of the implemented prototype.

Fig. 6(a) shows the output voltage and the primary current in the HFT when a reference change from 25 to 30 V is performed. It is observed that the voltage reaches its new reference value in 2 ms without any oscillations or overshoot, whereas the primary current in the HFT shows a transient given the reference change. However, the control strategy ensures to maintain its mean value at zero.

Fig. 6(b) shows the output voltage and the primary current in the HFT when a linear load change from 50 to 100 W is performed. In this case, the voltage decreases by approximately 3% with respect to the reference value, and it then returns to the reference value within 2 ms, whereas the primary current in the HFT shows a transient without oscillations or overshoot and maintains its mean value at zero.

Fig. 6(c) shows the output voltage and the primary current in the HFT when the 100 W linear load is disconnected and a 110 W CPL is connected. In this case, the output voltage shows a decrease lower than 3% with respect to the reference value, and it goes back to the reference value within 2 ms, whereas the primary current in the HFT shows a little overstepping but maintains its mean value at zero. In this case, it is observed that, even in the most unfavorable stability case, which takes place when the CPL is connected, both the output voltage and the primary current in the HFT show no oscillations and meet the established design specifications.

Fig. 8 shows the output voltage and the primary current of the HFT in a steady state, when there is a 100 W linear load connected to the converter and the output voltage is 30 V. It is observed that the controller is able to maintain the output voltage within the established reference value and it also ensures the mean value of the primary current of the HFT at zero.

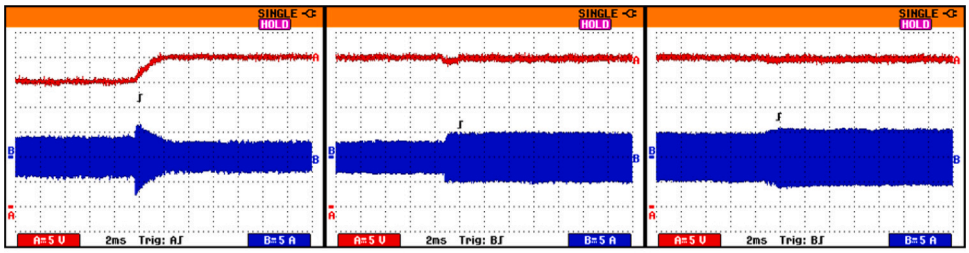

Fig. 6. Performance of the experimentally implemented DC–DC DAB converter. (a) Output voltage (red) and primary current of the HFT (blue) for a reference change, (b) output voltage (red) and primary current of the HFT (blue) for a load change from 50 to 100 W, (c) output voltage (red) and primary current of the HFT (blue) for the connection of a 110 W CPL.

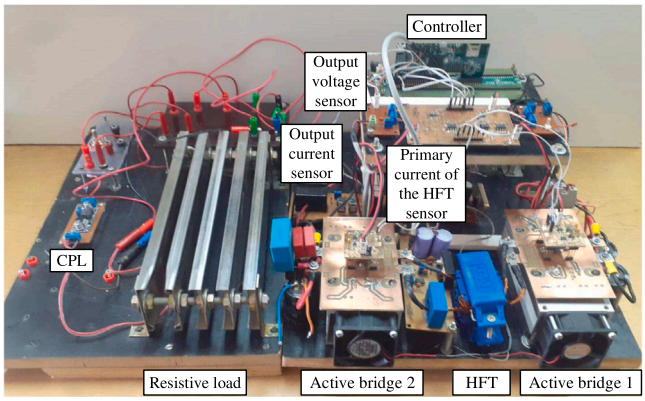

Fig. 7. Picture of the implemented laboratory prototype.

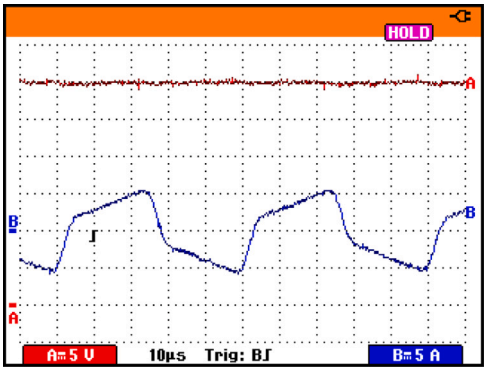

Fig. 8. Output voltage (red) and primary HFT current (blue) in a steady state.

Finally, to compare the performance of the proposed control strategy with a conventional one the test was repeated but using PI controllers, with the same setting as the one used in the simulation. This test is shown in Fig. 9, and it is observed that a lower performance is obtained compared to the proposed controller, since the output voltage presents overshoot and oscillations in the transient instants and a lower settling time. On the other hand, the primary current is maintained with zero mean value in steady state, although it presents transients with oscillations.

5. Conclusions

In this work, a control strategy was designed and implemented for a DC–DC DAB converter used to interconnect two feeders in a DC MG. The proposed strategy allows to regulate the output voltage of the converter according to a required reference value while maintaining the mean value from the primary and secondary currents of the HFT at zero.

Thanks to the decoupling carried out in the design of the controllers, it was possible to separate the GSSA model from the converter into two parts, which simplifies the design of both controllers and facilitates their implementation.

Given that the controllers are designed by means of a nonlinear control technique, an excellent dynamic performance is obtained, thus ensuring the system's stability against reference changes, large load variations, and even unfavorable stability cases such as the connection of CPL loads.

The performance of the proposed strategy is validated through simulation and experimental results, where the controller shows a good performance, being able to meet the established performance requirements, such as settling time and zero steady state error. In addition, the results obtained show that the controller allows ensuring the stability of the system, even when the CPL is connected, since it is observed that both the output voltage and the primary and secondary currents of the HFT do not present oscillations and manage to stabilize at their values steady state in the required settling time.

CRediT authorship contribution statement

Francisco D. Esteban: Conceptualization, Methodology, Software, Investigation. **Federico M. Serra:** Conceptualization, Methodology, Software, Investigation. **Cristian H. De Angelo:** Conceptualization, Methodology, Software, Investigation. **Oscar D. Montoya:** Conceptualization, Methodology, Software, Investigation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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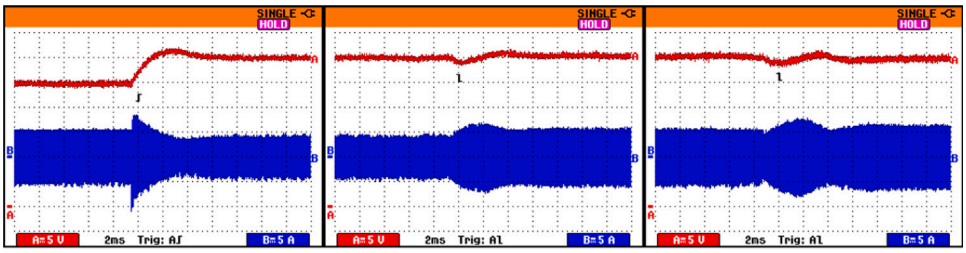

(a) (b) (c)

Fig. 9. Performance of the experimentally implemented DC–DC DAB converter with PI controller. (a) Output voltage (red) and primary current of the HFT (blue) for a reference change, (b) output voltage (red) and primary current of the HFT (blue) for a load change from 50 to 100 W, (c) output voltage (red) and primary current of the HFT (blue) for the connection of a 110 W CPL.

Appendix A

The GSSA model approximates a waveform $x(t)$ using the complex Fourier series [24], as follows,

$$x(t) = \sum_{k=-\infty}^{\infty} \langle x \rangle_k(t) e^{jk\omega t}, \tag{32}$$

where $\langle x \rangle_k(t)$ is the coefficient of the kth harmonic of the Fourier series, and it is defined by the sliding average over a switching period T_s [7],

$$\langle x \rangle_k = \langle x \rangle_{k_R} + j\langle x \rangle_{k_I} = \frac{1}{T_s} \int_{t-T_s}^{t} x(t) e^{-jk\omega t} dt, \tag{33}$$

where $T_s = 1/f_s$. From (32) and (33) two fundamental properties of GSSA modeling are obtained.

The first one describes the derivative of a state variable in terms of its Fourier coefficients given by (33) and their derivatives with respect to time,

$$\frac{d}{dt}\langle x \rangle_k(t) = \langle \frac{d}{dt} x \rangle_k(t) - jk\omega \langle x \rangle_k(t). \tag{34}$$

Whereas the second property denotes the kth average of the product between two variables $x(t)$ and $y(t)$ and can be obtained by discrete convolution [7],

$$\langle xy \rangle_k = \sum_{i=-\infty}^{\infty} \langle x \rangle_{k-i} \langle y \rangle_i \tag{35}$$

Appendix B

In the extraction of the GSSA components, the scheme shown in Fig. 10 [24] is used. Obtaining the real and imaginary parts (x_2 and x_3 respectively) of the fundamental component of the primary current of the HFT is done through a demodulation process followed by low-pass filtering. Whereas the DC component of the HFT primary current (x_4), is obtained from a low-pass filtering process.

Here, n is a discrete variable denoting the current sample of the primary current of the HFT, while N is the number of samples of the recursive low-pass filter.

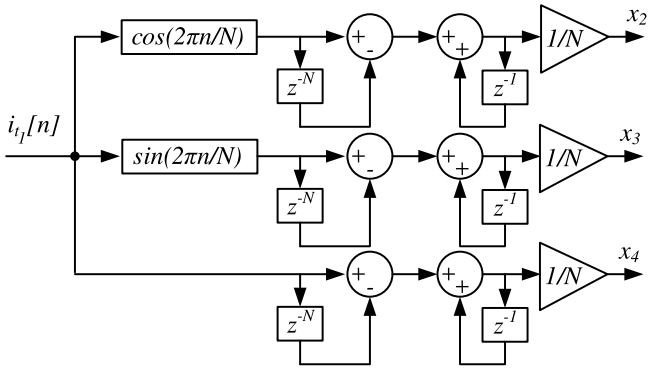

Fig. 10. Recursive filter for the extraction of the GSSA components.

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