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Photovoltaic System for Microinverter Applications Based on a Non-Electrolytic-Capacitor Boost Converter and a Sliding-Mode Controller

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Abstract: This paper presents a photovoltaic (PV) system designed to reduce the DC-link capacitance present in double-stage PV microinverters without increasing the capacitor interfacing the PV source. This solution is based on a modified boost topology, which exhibits continuous current in both input and output ports. Such a characteristic enables the implementation of PV microinverters without electrolytic capacitors, which improves the reliability in comparison with solutions based on classical converters with discontinuous output current and electrolytic capacitors. However, the modified boost converter exhibits different dynamic behavior in comparison with the classical boost converter; thus, design processes and controllers developed for the classical boost converter are not applicable. This paper also introduces a sliding-mode controller designed to ensure the stable operation of the PV microinverter around the maximum power point. Moreover, this solution also rejects the voltage oscillations at double the grid frequency generated by the grid-connection. The global stability of the complete PV system is formally demonstrated using mathematical analyses, and a step-by-step design process for both the power stage and control system is proposed. Finally, the design process is illustrated using a representative application example, and the correct operation of the PV system is validated using realistic circuital simulations. The results validate the accuracy of the theoretical equations proposed for both the design and control of the novel PV system, where errors below 4.5% were obtained for the ripple prediction, and below 1% for the prediction of the dynamic behavior.

Keywords: PV microinverter; sliding-mode controller; non-electrolytic capacitor; boost converter

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1. Introduction

Photovoltaic (PV) installations are a growing market due to the objective of reducing greenhouse emissions by 2030 by, at least, 55% [1]. In addition, PV installations can be used to replace backup diesel generations, reducing urban pollution in large cities. Additional benefits of PV systems are the availability of solar energy at the production site, avoiding the need of fuel transportation required by traditional diesel generators; better usability of large surfaces such as rooftops; and simple scalability of the PV power generation.

In addition to the modularity, PV installations also require mitigation of the detrimental effect of the partial shading conditions on series-connected PV panels (named strings), in which small shades could significantly reduce the power production [2]. One suitable solution to mitigate this problem is to introduce voltage equalizers [2,3], which provide a path for the current difference between two (or more) series-connected modules. This solution avoids the activation of the bypass diode associated to the shaded module; otherwise, such a module will operate in short-circuit condition without producing power.

Those voltage equalizers can be designed with classical inductor switched topologies or using switched capacitor solutions [2], which reduce the converter size and electromagnetic pollution [4–7] but introduce discontinuous input or output currents. However, since the voltage equalizers are designed to interact with series-connected modules, introducing (or subtracting) modules from the PV installation requires a disconnection of the whole string. Finally, voltage equalizers do not introduce a voltage boosting factor; hence, several PV modules must be connected in series to reach the input voltage needed by classical grid-connected inverters.

Another strategy to mitigate the effect of partial shading conditions, and to provide modularity to the PV installation, concerns the use of microinverters [8]. Those devices enable to easily increase (or decrease) the PV installation depending on changes in the load demand without major changes in the installed devices. Moreover, the microinverter avoids the series connection of PV modules; hence, no bypass diodes are activated, which reduces the impact of partial shading conditions. The classical two-stage microinverter is a small power system formed by a PV module, a first stage to perform the tracking of the maximum power point (MPPT) and the regulation of the PV voltage, and a second stage in charge of the grid synchronization and the regulation of the DC-link between both stages; such a microinverter structure is observed in Figure 1.

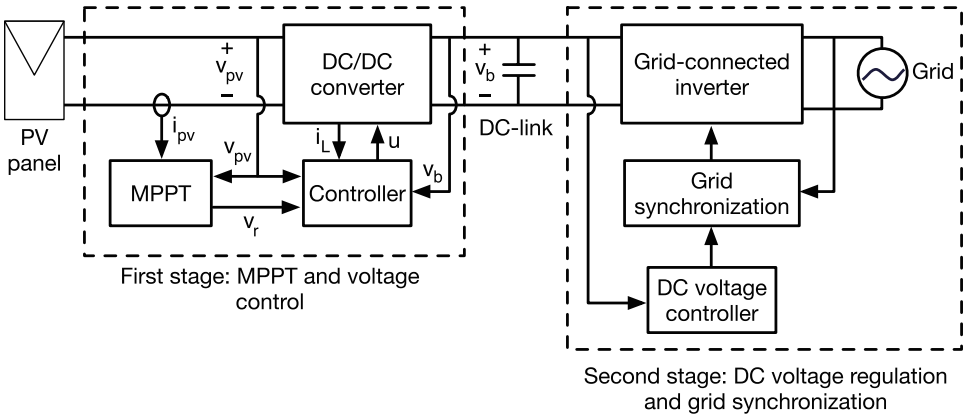

Figure 1. Structure of a PV microinverter with DC-link regulation and grid connection.

The first stage of the microinverter includes a DC/DC converter to match the PV voltage with the DC-link voltage, as reported in [8,9], where that DC/DC converter must be regulated to track the maximum power point (MPP) of the PV source in a particular environmental condition. Such a control system is formed by two components [9]: an MPPT algorithm, which defines the optimal PV voltage reference v_r, and a high-bandwidth controller, to ensure that the PV voltage v_{pv} follows the MPPT reference. The MPPT algorithm usually requires the measurement of the PV voltage and current, v_{pv} and i_{pv}, while the controller could require the measurement of additional internal variables of the DC/DC converter such as the inductor current i_L or DC-link voltage v_b. Finally, the controller generates the control signal u of the DC/DC converter.

The grid connection is performed using an inverter, which has two main objectives: interact with the grid to deliver the PV power, and regulate the DC-link voltage. This last objective is very important in PV systems, since the grid interaction forces a single-phase inverter to inject sinusoidal power at double the grid frequency, which produces a sinusoidal voltage oscillation at double the grid frequency in the DC-link. This problem is clearly explained in [10], where it is demonstrated that such a DC-link voltage oscillation can be translated into the PV voltage, making the MPPT algorithm unstable and avoiding the extraction of the maximum power. In addition, the average value of the DC-link must be regulated to avoid non-feasible operation conditions for the first-stage, e.g., high DC-link voltage that could destroy the DC/DC converter. Therefore, the inverter of the second-stage

must regulate the average value of the DC-link voltage, as reported in [11], where the size of the capacitor defines two main aspects of the DC-link:

- The amplitude of the low-frequency voltage oscillations at double the grid frequency, which introduce a perturbation on the first stage, as discussed in [10]; thus, the controller of the first stage must be designed to avoid the transmission of such a DC-link perturbation into the PV voltage.
- The magnitude of the high-frequency voltage ripple generated by the DC/DC converter of the first stage, which introduces high-frequency current harmonics into the second-stage inverter. The current harmonics deteriorate the power quality provided to the inverter, introducing high-frequency noise that could interfere with the inverter control system and sensing circuits.

With the aim of reducing the previous problems, high capacitances are usually adopted to design the DC-link, requiring electrolytic capacitors. For example, the microinverters reported in [12,13] consider DC-link capacitors of 2200 μF, which is clearly in the electrolytic range. Since electrolytic capacitors have a much higher failure rate in comparison with other technologies such as film capacitors [10], using large DC-link capacitors introduces a reliability problem to the PV microinverter.

1.1. Literature Review

This subsection discusses different approaches, reported in literature, to face the previous considerations.

The microinverter reported in [8] adopts a DC/DC boost converter for the first stage, which provides the boosting factor needed to match the PV voltage and the DC-link voltage. The first stage has no high-frequency controller; hence, the boost converter can be perturbed by the low-frequency oscillations present in the DC-link, and no global stability of the first stage is ensured. Finally, this solution adopts an incremental conductance (INC) MPPT algorithm. The microinverter presented in [12] is also based on an open-loop boost converter with no global stability ensured; however, in this case, a large electrolytic capacitor is used to reduce the DC-link voltage oscillations at the expense of reliability; finally, the perturb and observe (P&O) MPPT algorithm is used to maximize the power production. The work reported [14] also considers a grid-connected PV system; the first stage of this solution is formed by a boost converter in open-loop with a capacitive DC-link, where the duty cycle is defined by a predictive MPPT algorithm. In this case, the voltage oscillations at the DC-link are mitigated by using a three-phase inverter, which requires balanced power flows in each phase to ensure a small oscillation magnitude. Since three-phase networks are not common in urban/residential power systems, this solution is restricted to industrial environments. Finally, the design of the power stage is not discussed.

Another approach is reported in [9], where a flyback converter is adopted. The first stage of this solution includes a sliding-mode controller (SMC) to mitigate the DC-link voltage oscillations, thus avoiding the need for large electrolytic capacitors. However, the flyback converter requires the use of a high-frequency transformer, which introduces electromagnetic pollution that could affect the sensors of the system. Instead, the work reported in [15] adopts both the boost converter and SMC into the first stage to ensure stability. The SMC is designed considering a resistive load to simplify the analysis. Despite changes on the resistive load being considered, such an approximation does not correctly represent the input of a grid-connected inverter; thus, no global stability can be ensured. In addition, the boost converter design is not analyzed; thus, no guidelines concerning the design of the passive elements are provided. Similar problems are found in [11], where an SMC is designed for the boost converter in the first stage, ensuring stability of both the converter and P&O MPPT algorithm, but the design of the power stage is not discussed.

The work reported in [16] succeeds in providing design equations for the first-stage converter (with a boost topology). As in the case of [15], a resistive load model is used to represent the second stage; thus, those results are not easily applicable to real PV microinverters. Moreover, the work reported in [16] adopts a robust-direct-adaptive controller

(RDAC), but the calculation of the controller parameters is not discussed. Finally, an MPPT algorithm similar to the P&O solution is adopted. The work discussed in [13] is also based on a boost converter, where the first stage is regulated using a mixed proportional–integral (PI)-P&O controller, but the system stability is not formally analyzed. Moreover, the converter design is not discussed. The solution reported in [17] is also based on a boost converter and an SMC; however, in this case, an additional PI controller is introduced. The main advantage of this solution is the use of a particle swarm optimization (PSO) to obtain the optimal controller parameters; however, the converter design is not discussed and the global stability of the system is not formally demonstrated. Finally, the work reported in [18] presents a first stage based on a boost converter controlled by an SMC and a P&O algorithm. This solution considers an accurate model for the DC-link, and the stability of the PV system is formally demonstrated. However, the design of the converter elements is not taken into account, and the output current of this first stage is discontinuous.

From the previous discussions, the following conclusions are obtained:

- The boost converter is the most widely adopted solution to develop PV microinverters. Nonetheless, a design procedure for the converter elements, based on the particular requirements of the PV installation, is needed.
- The SMC is widely adopted in PV systems due to its robustness to parametric changes and satisfactory rejection of environmental perturbations. However, the global stability is not ensured; thus, the associated mathematical analysis is needed.
- The low-frequency voltage oscillations at the DC-link, caused by the grid connection of the second stage, must be reduced or mitigated. This can be performed by implementing the DC-link with a large electrolytic capacitor at the expense of reliability or by using high-bandwidth controllers in the first stage.
- The solutions previously discussed are based on DC/DC converters with discontinuous output current, requiring large DC-link capacitors to reduce the high-frequency current harmonics introduced to the second stage.
- The P&O algorithm is the most widely used solution in PV microinverter applications due to its efficiency and simplicity, followed by the INC solution.

1.2. Contributions of the Proposed Solution

The solution proposed in this paper improves the first stage of PV microinverters by enabling the implementation of a non-electrolytic DC-link using a new approach: developing the first stage using a non-electrolytic-capacitor (NEC) boost converter, which provides continuous output current, thus decreasing the DC-link capacitor needed to reduce the high-frequency current harmonics introduced to the second stage. This approach uses the NEC boost converter with non-pulsating and ripple-free output current proposed in [19], which introduces an improved impedance network (over the Z-network of the classical boost converter) but without changing the voltage conversion ratio and keeping the continuous input current condition. In addition, the PV system based on the NEC boost topology is analyzed in detail to provide a mathematical model and a comprehensive design procedure.

Moreover, the operation complexity of the NEC boost converter requires a suitable control system to guarantee the global stability of the PV system; thus, an SMC is designed to regulate the NEC boost converter and to guarantee global stability to the PV installation. This proposed SMC also enables rejecting the low-frequency perturbations present in the DC-link due to the grid connection. Finally, the formal proof of the global stability is developed.

1.3. Manuscript Organization

The remainder of the paper is organized as follows. Section 2 presents a detailed analysis of the proposed PV system, describing the main objectives of the NEC boost converter into the PV system. Moreover, the non-linear model of the PV system is calculated. Section 3 describes the design of the SMC including the mathematical analyses needed

to provide global stability. This section also describes the practical implementation of the SMC using an analog circuit.

Section 4 proposes a method to design the dynamic behavior of the PV system, based on a cascade voltage controller, which is needed to ensure the stability of the MPPT algorithm. In addition, the implementation of the complete control structure is summarized in a block diagram. Then, Section 5 illustrates the design procedure using a realistic application example, which includes the calculation of the parameters for both the NEC boost converter and SMC, including the verification of the global stability equations. Section 6 presents the validation of the theoretical analyses using realistic and detailed circuital simulations in the commercial power electronics simulator PSIM [20], which is used in literature to validate theoretical expressions developed for design and control of other PV microinverters; examples of such validations are reported in [9,21]. Finally, the conclusions close the paper.

2. Description the PV System Based on the NEC Boost Converter

The circuital description of the proposed PV system, based on the NEC boost converter, is presented in Figure 2. Such a circuit models the second stage of the microinverter using the voltage source v_b, which is an acceptable model taking into account that the grid-connected inverter has a control loop to ensure a stable average voltage in the DC-link. However, the sinusoidal power injection into the grid produces a sinusoidal voltage in v_b at the double of the grid frequency, which is added to the average value of v_b as an additional perturbation. The circuit also shows the measurement of the PV current and voltage because both are needed to perform the MPPT action; in this work, it is considered the P&O algorithm, but any other MPPT algorithm can be adopted.

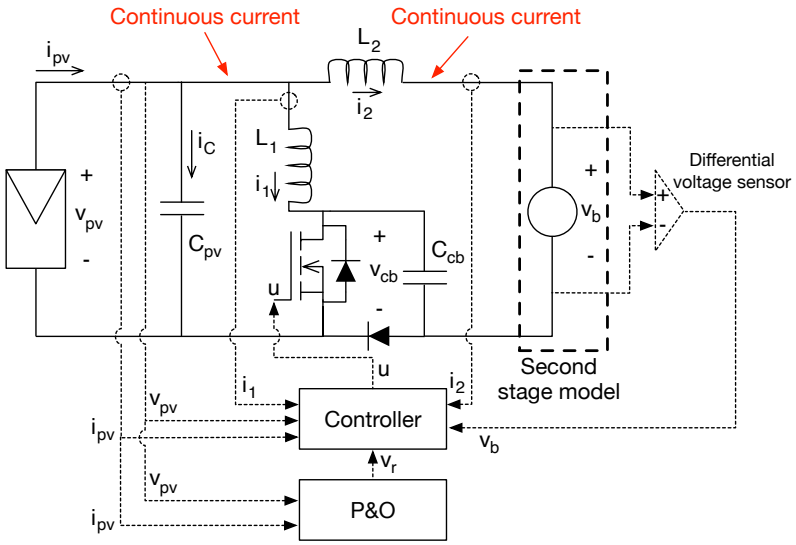

Figure 2. Circuital description of the PV system based on the NEC boost converter.

The input capacitor C_{pv} is added to the NEC boost converter proposed in [19], which is used to set the operation voltage to the PV source. Moreover, the converter has two inductors, L_1 and L_2, which are used to impose continuous current to both the input capacitor and output port, i.e., to the grid-connected inverter. Such a characteristic has two main purposes:

- Ensure a small voltage ripple to the PV voltage to reduce deviations from the MPP, thus ensuring a high efficiency of the MPPT algorithm.
- Introduce small current ripples to the DC-link of the second stage, which ensures a correct operation of the grid-connected inverter.

The NEC boost converter also has an internal capacitor C_{cb}, which is needed to ensure the continuous current condition at the output port as it will be explained afterwards. Finally, the converter has a MOSFET and a diode, which are complementarily activated.

The controller of the proposed PV system is designed so as to ensure a correct tracking of the reference v_r defined by the P&O algorithm, thus ensuring that the PV voltage v_{pv} is always at the optimal value. Such a controller also requires the measurement of both inductor currents i_1 and i_2; the measurement of the output voltage v_b; and the values of the PV voltage and current v_{pv} and i_{pv}, respectively, which are also needed to process the P&O algorithm.

2.1. Mathematical Model

The operation of the NEC boost converter, when the MOSFET is activated ($u = 1$), produces Topology 1, depicted at the top of Figure 3. The figure shows that the connection of the MOSFET imposes the voltage of C_{cb} capacitor (v_{cb}) into the diode, thus reverse-biasing the diode to deactivate it. Moreover, in this topology, the C_{cb} capacitor provides a path for the output current, which corresponds to the L_2 current i_2, ensuring a continuous current condition. Finally, it is evident that the output current of Node A is equal to the sum of the inductor currents ($i_1 + i_2$), thus imposing a continuous input current to the NEC circuit. Then, the differential equations describing the dynamic behavior of both inductor currents i_1 and i_2, the internal capacitor voltage v_{cb}, and the PV voltage v_{pv} are as follows:

$$\frac{di_1}{dt} = \frac{v_{pv}}{L_1} \tag{1}$$

$$\frac{di_2}{dt} = \frac{v_{pv} + v_{cb} - v_b}{L_2} \tag{2}$$

$$\frac{dv_{cb}}{dt} = \frac{-i_2}{C_{cb}} \tag{3}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - (i_1 + i_2)}{C_{pv}} \tag{4}$$

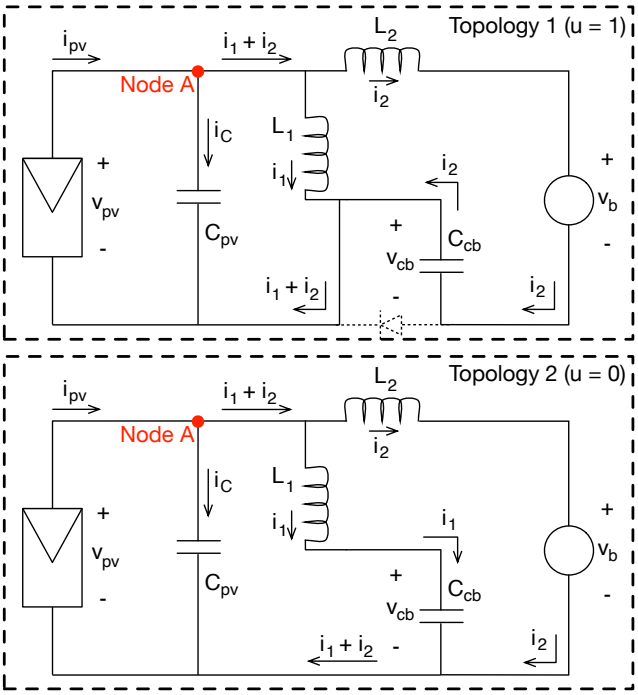

Figure 3. Topologies of the PV system based on the NEC boost converter.

When the MOSFET is deactivated ($u = 0$), Topology 2 occurs, which is depicted at the bottom of Figure 3. In this topology, the C_{cb} capacitor provides a path for the current of L_1; however, in this case, the diode is activated by the combined current flow of $i_1 + i_2$. Finally, as in topology 1, the output current of Node A is equal to the sum of the inductor currents

$(i_1 + i_2)$, imposing a continuous input current to the NEC circuit. The differential equations describing the dynamic behavior in this second topology are as follows:

$$\frac{di_1}{dt} = \frac{v_{pv} - v_{cb}}{L_1} \tag{5}$$

$$\frac{di_2}{dt} = \frac{v_{pv} - v_b}{L_2} \tag{6}$$

$$\frac{dv_{cb}}{dt} = \frac{i_1}{C_{cb}} \tag{7}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - (i_1 + i_2)}{C_{pv}} \tag{8}$$

Then, the switched model of the system is obtained by combining the differential equations for both topologies using the control signal of the MOSFET (u) as follows:

$$\frac{di_1}{dt} = \frac{v_{pv} - v_{cb} \cdot (1 - u)}{L_1} \tag{9}$$

$$\frac{di_2}{dt} = \frac{v_{pv} - v_b + v_{cb} \cdot u}{L_2} \tag{10}$$

$$\frac{dv_{cb}}{dt} = \frac{i_1 \cdot (1 - u) - i_2 \cdot u}{C_{cb}} \tag{11}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - (i_1 + i_2)}{C_{pv}} \tag{12}$$

Another useful representation corresponds to the averaged model, which averages the control signal u within the switching period T_{sw}, as given in (13). Therefore, the average dynamic behavior of both currents and voltages is modeled using (14)–(17).

$$d = \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} u \, dt \tag{13}$$

$$\frac{di_1}{dt} = \frac{v_{pv} - v_{cb} \cdot (1 - d)}{L_1} \tag{14}$$

$$\frac{di_2}{dt} = \frac{v_{pv} - v_b + v_{cb} \cdot d}{L_2} \tag{15}$$

$$\frac{dv_{cb}}{dt} = \frac{i_1 \cdot (1 - d) - i_2 \cdot d}{C_{cb}} \tag{16}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - (i_1 + i_2)}{C_{pv}} \text{ , where } i_1 \text{ is calculated from (14) and } i_2 \text{ from (15)} \tag{17}$$

The steady-state relations between the previous signals are calculated by assuming equal to zero the previous differential Equations (14)–(17), which leads to the following low-frequency expressions:

$$i_{pv} = i_1 + i_2 \tag{18}$$

$$v_{cb} = v_b \tag{19}$$

$$v_{pv} = (1 - d) \cdot v_b \tag{20}$$

$$(1 - d) \cdot i_1 = d \cdot i_2 \tag{21}$$

$$d = 1 - \frac{v_{pv}}{v_b} \tag{22}$$

Another important analysis concerns the calculation of current and voltage ripples in both the inductors and capacitors produced by the switching operation, which are calculated from the expressions on topology 1, as follows:

$$\delta i_1 = \frac{v_{pv} \cdot d \cdot T_{sw}}{2 \cdot L_1} \tag{23}$$

$$\delta i_2 = \frac{v_{pv} \cdot d \cdot T_{sw}}{2 \cdot L_2} \tag{24}$$

$$\delta v_{cb} = \frac{i_{pv} \cdot d \cdot (1-d) \cdot T_{sw}}{2 \cdot C_{cb}} \tag{25}$$

In the above expressions, δi_1 is the current ripple in i_1, δi_2 is the current ripple in i_2, and δv_{cb} is the voltage ripple in C_{cb}. The voltage ripple in C_{pv} is calculated by using the second-order filter expression in Node A, as reported in [22], which results in the following equation for the ripple δv_{pv}:

$$\delta v_{pv} = \frac{(\delta i_1 + \delta i_2) \cdot T_{sw}}{8 \cdot C_{pv}} \tag{26}$$

Finally, the voltage and current stresses on the semiconductor are also calculated. From the first topology in Figure 3, the voltage supported by the MOSFET is calculated as given in (27) and the current supported by the diode as given in (28). Similarly, from the second topology, the current supported by the MOSFET is calculated as given in (29) and the voltage supported by the diode as given in (30).

$$V_{MOS} = v_{cb} = v_b \tag{27}$$

$$I_D = i_1 + i_2 \tag{28}$$

$$I_{MOS} = i_1 + i_2 \tag{29}$$

$$V_D = -v_{cb} = -v_b \tag{30}$$

2.2. Comparison with the Classical Boost Converter

PV systems with a first stage based on the classical boost converter, similar to the one reported in [12], have the structure depicted in Figure 4. Such a circuit provides continuous input current; hence, the same input capacitor C_{pv} used in the NEC boost PV system can be adopted in this classical boost alternative to provide a fair comparison.

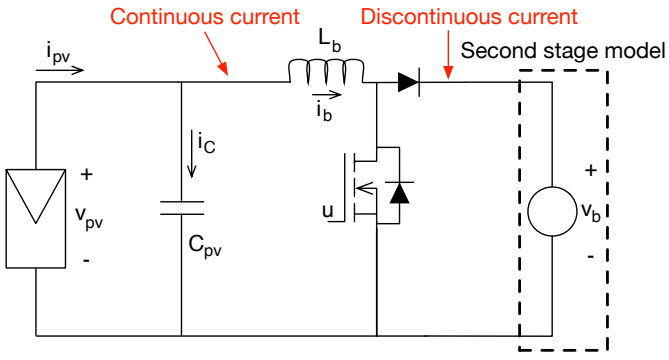

Figure 4. PV system based on the classical boost converter.

The switched model of this classical boost PV system is given in Equations (31) and (32), where the strong difference with the PV system based on the NEC boost converter is evident due to the difference with the switched Equations (9)–(12). Design procedures and controllers previously developed for the classical boost converter are not applicable to the

PV system based on the NEC boost converter; thus, new design and control analyses must be developed.

$$\frac{di_{L_b}}{dt} = \frac{v_{pv} - v_b \cdot (1-u)}{L_b} \tag{31}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - i_{L_b}}{C_{pv}} \tag{32}$$

A fair comparison between PV systems based on both the NEC and classical boost converters also requires providing the same PV voltage ripple—in the case of the classical boost converter, given in (33)—while the current ripple δi_{L_b} in the classical boost inductor is given in (34).

$$\delta v_{pv} = \frac{\delta i_{L_b} \cdot T_{sw}}{8 \cdot C_{pv}} \tag{33}$$

$$\delta i_{L_b} = \frac{v_{pv} \cdot d \cdot T_{sw}}{2 \cdot L_b} \tag{34}$$

For the sake of simplicity, the comparison between the NEC and classical boost PV systems considers both NEC inductors equal ($L_1 = L_2$), and the duty cycle is selected as $d = 0.5$ for both DC/DC converters. Then, analyzing Equations (26) and (33) shows that the same PV voltage ripple is achieved when $\delta i_{L_b} = (\delta i_1 + \delta i_2) = 2 \cdot \delta i_1$ since $\delta i_1 = \delta i_2$ because $L_1 = L_2$. From Equations (23) and (34), it is obtained that $L_b = L_1/2$ achieves the same PV voltage ripple.

However, the average current of the classical boost inductor, obtained from considering the differential Equation (32) equal to zero, is $i_{L_b} = i_{pv}$. Therefore, in the classical boost PV system, the inductor must support the complete PV current, while in the NEC boost PV system both inductors share the PV current, as observed in (18); in fact, for $d = 0.5$, both NEC inductors support half of the PV current ($i_1 = i_2 = i_{pv}/2$). In conclusion, the classical boost inductor has half of the inductance value but supports double the current in comparison with the NEC boost inductors. Then, a suitable way to contrast the inductance requirement of both PV systems is to compare the energy stored in the inductors: the energy stored in an inductor is $E_L = \frac{1}{2} \cdot L \cdot I^2$, where I is the current of the inductor. Applying the previous analysis to the classical boost PV system results in $E_b = \frac{1}{2} \cdot L_b \cdot i_{pv}^2 = \frac{1}{4} \cdot L_1 \cdot i_{pv}^2$; for the NEC boost PV system, the energy stored in each inductor is $E_1 = \frac{1}{2} \cdot L_1 \cdot \left(\frac{i_{pv}}{2}\right)^2 = \frac{1}{8} \cdot L_1 \cdot i_{pv}^2$, resulting in a total energy stored in both inductors $E_{L,NEC} = \frac{1}{4} \cdot L_1 \cdot i_{pv}^2$, which is the same energy stored in the inductor of the classical boost converter. Therefore, both PV systems require similar inductance storage.

Figure 4 shows that the classical boost PV system provides a discontinuous conduction current to the second stage, which corresponds to the diode current i_d. Figure 2 shows that the NEC boost PV system instead provides a continuous current to the second stage. The quantification of this difference can be performed using three measurements: the DC current expected by the second stage i_{dc}, the RMS current provided by the first stage, and the resulting AC current. The DC current is simple to calculate, since for a fair comparison both systems are considered operating with the same input current i_{pv} and voltage v_{pv}, and the same output voltage v_b. For this comparison, $d = 0.5$; thus, $i_{dc} = i_{pv}/2$ and $v_{pv} = v_b/2$.

The RMS currents are calculated as $\sqrt{\frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} i \, dt}$, where i must be replaced by the output currents of the PV systems, i.e., $i = i_d$ for the classical boost system and $i = i_2$ for the NEC boost system. Figure 5 shows the waveforms of the output currents for both PV

systems, which enables defining the expressions of those waveforms as (35) for i_d (classical boost) and (36) for i_2 (NEC boost).

$$i_d = \begin{cases} 0 & \text{for} \quad 0 \leq t < \frac{T_{sw}}{2} \\ -\frac{4 \cdot \delta i_{L_b}}{T_{sw}} \cdot t + \left(i_{pv} + \delta i_{L_b} \right) & \text{for} \quad \frac{T_{sw}}{2} \leq t < T_{sw} \end{cases} \tag{35}$$

$$i_2 = \begin{cases} \frac{4 \cdot \delta i_2}{T_{sw}} \cdot t + \left(\frac{i_{pv}}{2} - \delta i_2 \right) & \text{for} \quad 0 \leq t < \frac{T_{sw}}{2} \\ -\frac{4 \cdot \delta i_2}{T_{sw}} \cdot t + \left(\frac{i_{pv}}{2} + \delta i_2 \right) & \text{for} \quad \frac{T_{sw}}{2} \leq t < T_{sw} \end{cases} \tag{36}$$

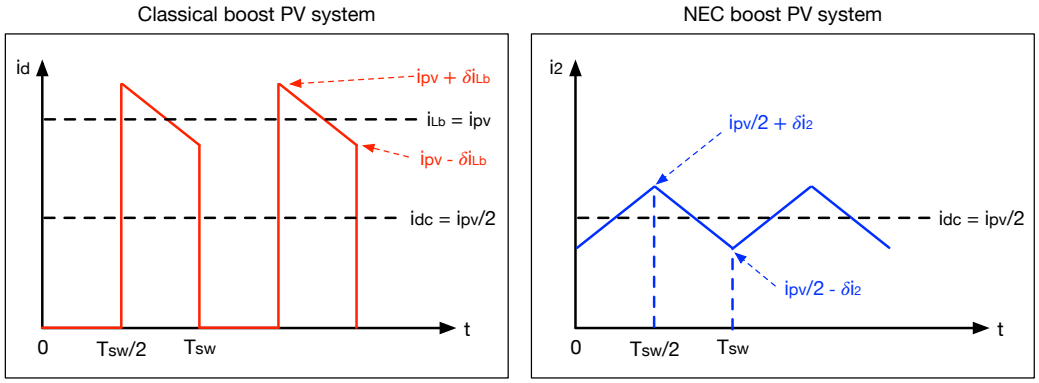

Figure 5. Waveforms of the output currents of classical boost and NEC boost PV systems ($d = 0.5$).

Taking into account that $\delta i_{L_b} = 2 \cdot \delta i_1 = 2 \cdot \delta i_2$ for this comparison ($d = 0.5$), the RMS values for i_d (classical boost) and i_2 (NEC boost) are given in (37) and (38), respectively.

$$i_{RMS,d} = \sqrt{\frac{2 \cdot \delta i_2^2}{3} + \frac{i_{pv}^2}{2}} \tag{37}$$

$$i_{RMS,2} = \frac{\sqrt{3}}{6} \cdot \sqrt{4 \cdot \delta i_2^2 + 3 \cdot i_{pv}^2} \tag{38}$$

Diving the RMS expression for the classical boost (37) into the RMS expression for the NEC boost (38) results in a constant relation equal to $\sqrt{2}$. This means that the RMS value of the output current provided by the classical boost converter is 41.4% higher than the RMS current provided by the NEC boost converter, which produces higher power losses on the elements of the second stage.

Moreover, the AC components of the output currents can be calculated from $i_{RMS}^2 = i_{dc}^2 + i_{ac}^2$. In this way, expression (39) provides the AC component of the output current introduced into the second stage by the classical boost solution, while expression (40) reports the AC components generated by the NEC boost solution. Those AC components introduce undesired current harmonics to the second stage, which perturb the control system and degrade the power quality of the DC-link. In fact, since the PV system produces DC power, any AC component is useless, and the presence of those AC components increment the power losses (due to the ohmic effect) and perturb both the control systems and measurement devices.

$$i_{ac,d} = \sqrt{\frac{2 \cdot \delta i_2^2}{3} + \frac{i_{pv}^2}{4}} \tag{39}$$

$$i_{ac,2} = \frac{\delta i_2}{\sqrt{3}} \tag{40}$$

The magnitude of those undesired AC components are contrasted by dividing the AC component produced by the classical boost solution (39) with the AC component produced

by the NEC boost solution (40). Such an analysis is performed for different values of the current ripple δi_2 (as percentage of the DC value $i_2 = i_{pv}/2$), and the results are reported in Figure 6. Those results put into evidence the significant increment in the current harmonics introduced by the classical boost converter in comparison with the NEC converter: for an inductor current ripple of 5%, the classical boost PV system introduces an AC component 34.67 times higher than the NEC boost PV system; for an inductor current ripple of 20%, such a relation drops to 8.76 times, but the NEC boost PV system still introduces an AC component much smaller.

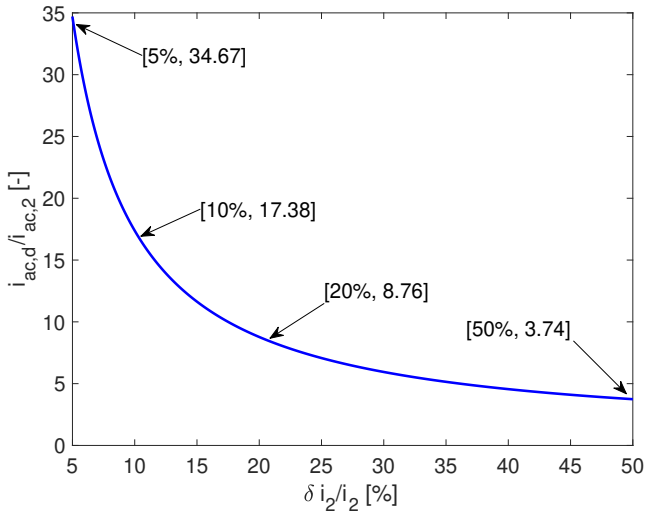

Figure 6. Comparison of the AC components introduced into the second stage by both the classical and NEC boost solutions ($d = 0.5$).

In conclusion, the proposed PV system based on the NEC boost converter introduces lower current harmonics in comparison with a PV system based on the classical boost converter, thus providing a better power quality to the DC-link or gird-connected inverter. Moreover, the NEC boost PV system can be designed to exhibit the same PV voltage ripple provided by the classical boost solution with an equivalent inductive energy storage, which provides a fair comparison between both solutions.

Other DC/DC converters can also be used to provide continuous input and output currents in a PV system, but with different voltage conversion ratio, voltage polarity, or stress in the elements. For example, the Cuk converter provides continuous current at both the input and output ports [23], but in a PV system application, the input inductor of the Cuk converter must support all the PV current, while the inductors of the NEC boost converter only support part of the PV current. Similarly, the internal capacitor voltage of the Cuk converter is higher than the output voltage (v_b/d); in fact, for the condition used in this comparison section ($d = 0.5$), the internal capacitor of the Cuk converter must support 50% more voltage than the internal capacitor of the NEC boost converter (which only supports the output voltage). Moreover, the output voltage of the Cuk converter has inverted polarity, which introduces additional complexity to the sensor circuits with respect to the classical boost converter. However, the output of the NEC boost converter has a voltage with a different reference with respect to the PV source, which requires an additional differential voltage sensor, similar to the Cuk converter, as depicted in Figure 2.

Finally, the advantage of reaching the MPP condition when the output voltage is near or lower than the PV voltage, provided by buck/boost-type converters [24], does not apply to microinverter applications since the input voltage required by the inverter of the second stage is much higher than the PV voltage provided by a small PV source. For example, a BP585 PV panel has a maximum MPP voltage equal to 18 V, while some boost inverters require a DC-link voltage equal to 48 V; more traditional buck inverters require input voltages higher than 160 V for connection to 110 VAC grids and input voltages higher than

312 V for connection to 220 VAC grids. Therefore, for microinverter applications, the NEC boost converter provides lower component stress and simpler sensing conditions than the Cuk converter without a significant disadvantage.

3. Sliding-Mode Controller

The correct operation of the PV system based on the NEC boost converter requires the following conditions:

1. Stable operation of the NEC boost converter, which requires a stable v_{cb} voltage; hence, the stable relation between the inductor currents given in (21) must be ensured, i.e., $(1-d)\cdot i_1 = d\cdot i_2$.
2. The regulation of the PV voltage is needed to impose the MPPT reference to the PV panel. In this case, it is proposed to regulate the PV current first, which corresponds to the input current of the NEC boost converter. An additional voltage controller will be designed, which will generate the current reference needed to regulate the PV voltage.

Then, a sliding-mode controller (SMC) is designed to provide robustness and global stability for any feasible operation condition of the PV system. The first step to design the SMC is to define the switching function, which establishes the SMC sliding surface. Based on the previous two control requirements, the switching function given in (41) is proposed. The first component of the switching function (left) imposes the stable relation between the inductor currents, while the second component (right) forces the PV current i_{pv} to follow the desired reference i_r.

$$\psi = \underbrace{\left[i_1\cdot(1-d) - i_2\cdot d\right]}_{\text{1. Inductor current balance}} + \underbrace{\left[\left(i_1+i_2-i_{pv}\right) - i_r\right]}_{\text{2. Input current control}} \tag{41}$$

The stability analysis of SMC for switching converters requires three analytical tests [25]—transversality condition, reachability conditions, and equivalent control; these analyses are provided in the following subsections.

3.1. Transversality Analysis

The transversality analysis requires the switching function derivative, which is calculated as given in (42), where $\frac{di_1}{dt}$ and $\frac{di_2}{dt}$ were replaced from (9) and (10), respectively. Moreover, $\frac{di_{pv}}{dt}$ is PV current derivative produced by the environmental conditions, and $\frac{di_r}{dt}$ is the derivative of the reference signal.

$$\frac{d\Psi}{dt} = (2-d)\cdot\left[\frac{v_{pv} - v_{cb}\cdot(1-u)}{L_1}\right] + (1-d)\cdot\left[\frac{v_{pv} - v_b + v_{cb}\cdot u}{L_2}\right] - \frac{di_{pv}}{dt} - \frac{di_r}{dt} \tag{42}$$

The transversality condition evaluates the ability of the SMC to change the trajectory of the switching function; thus, this condition tests the presence of the control signal in the switching function derivative. The mathematical formulation of this test is as follows [25]:

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) \neq 0 \tag{43}$$

Replacing the expression of the switching function derivative (42) into the transversality condition (43) leads to:

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = (2-d)\cdot\frac{v_{cb}}{L_1} + (1-d)\cdot\frac{v_{cb}}{L_2} > 0 \tag{44}$$

The previous transversality value is always positive because $L_1 > 0$, $L_2 > 0$, $d < 1$ and $v_{cb} > 0$; thus, it is different from zero. Therefore, expression (44) confirms the transversality condition is always fulfilled.

3.2. Reachability Analysis

The reachability conditions evaluate the capability of the controller to reach the desired surface (i.e., desired behavior) from any arbitrary operation condition. Figure 7 shows a graphical representation of the reachability conditions: when the switching function Ψ is operating above the desired surface (i.e., $\Psi > 0$), the switching function derivative must be negative (i.e., $\frac{d\Psi}{dt} < 0$) to reach the desired surface $\Psi = 0$; similarly, when the switching function is operating below the desired surface (i.e., $\Psi < 0$), the switching function derivative must be positive (i.e., $\frac{d\Psi}{dt} > 0$) to reach the surface.

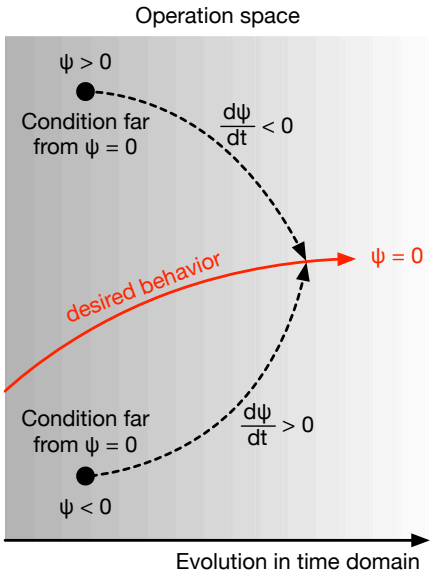

Figure 7. Derivation of the reachability conditions.

The analysis of the reachability conditions also requires defining the conditions of the control signal u to produce the desired sign on the switching function derivative. Such an analysis is performed using the sign of the transversality value (44): in this case, the transversality value is positive, which means that a positive value of the control signal ($u = 1$) produces a positive sign on the switching function derivative, while $u = 0$ produces a negative sign on the same derivative. Therefore, those reachability conditions can be mathematically expressed as follows:

$$\lim_{\Psi \to 0^+} \left. \frac{d\Psi}{dt} \right|_{u=0} < 0 \tag{45}$$

$$\lim_{\Psi \to 0^-} \left. \frac{d\Psi}{dt} \right|_{u=1} > 0 \tag{46}$$

Evaluating the theoretical reachability conditions (45) and (46) using the expression for the switching function derivative (42) leads to the following dynamic restrictions for the reference signal:

$$\frac{di_r}{dt} < (2-d) \cdot \frac{v_{pv}}{L_1} + (1-d) \cdot \frac{v_{pv}}{L_2} - \frac{di_{pv}}{dt} \tag{47}$$

$$\frac{di_r}{dt} > (2-d) \cdot \frac{v_{pv} - v_b}{L_1} + (1-d) \cdot \frac{v_{pv} - v_b}{L_2} - \frac{di_{pv}}{dt} \tag{48}$$

Therefore, those dynamic restrictions must be fulfilled to ensure the stability of both the proposed SMC and PV system.

3.3. Equivalent Control Condition

The equivalent control condition evaluates the capability of the controller to force the switching function to remain operating inside the surface. This analysis is performed by calculating the equivalent control signal u_{eq}, which corresponds to the average value of the control signal u, and such an equivalent value u_{eq} must be trapped into the values of u [9]. In particular, for switching converters, u_{eq} is equal to the duty cycle as reported in (13); thus, this analysis evaluates the saturation of the duty cycle:

$$0 < u_{eq} = d < 1 \tag{49}$$

Since this condition is evaluated inside the surface, $\Psi = 0$ and $\frac{d\Psi}{dt} = 0$. Those conditions formalize the stable trajectory of the switching function: inside the surface and with a parallel trajectory, i.e., always equal to the desired behavior. Then, substituting (42) into (49) produces the following equivalent control value:

$$u_{eq} = d = \frac{\frac{di_r}{dt} + \frac{di_{pv}}{dt} - (2-d)\cdot\frac{v_{pv}-v_b}{L_1} - (1-d)\cdot\frac{v_{pv}-v_b}{L_2}}{(2-d)\cdot\frac{v_b}{L_1} + (1-d)\cdot\frac{v_b}{L_2}} \tag{50}$$

Finally, evaluating the saturation limits defined in (49) using the u_{eq} expression given in (50) produces the same dynamic restrictions for $\frac{di_r}{dt}$ given in (47) and (48). In conclusion, the global stability of the SMC is ensured when the dynamic restrictions (47) and (48) are fulfilled.

3.4. Practical Implementation

The theoretical conceptualization of the SMC considers the switching function Ψ sliding around the surface $\Psi = 0$. This behavior is imposed by the reachability conditions (45) and (46), both ensured in (47) and (48): when Ψ is below 0, the SMC forces a positive derivative in Ψ, driving Ψ to 0; however, Ψ continues increasing and becomes positive. At that moment, the SMC forces a negative derivative in Ψ, driving Ψ to 0. That derivative change occurs at the instant in which Ψ crosses 0, producing an unlimited switching frequency that introduces high-frequency harmonics to the system, which could damage the MOSFETs.

The previous problem is solved by limiting the switching frequency in agreement with the MOSFET specifications. This limitation is performed by introducing a hysteresis band around $\Psi = 0$, where the bandwidth defines the maximum switching frequency. Figure 8 illustrates the effect of the hysteresis band, where a larger hysteresis width H produces a longer switching period T_{sw}, thus reducing the switching frequency $F_{sw} = 1/T_{sw}$. Moreover, since the switching function derivative is a finite number (42), Figure 8 shows that the hysteresis band imposes a limited switching frequency.

The introduction of the hysteresis band imposes the practical control law that must be implemented, which is also observed in Figure 8, as follows:

$$u = \begin{cases} \text{change to ON (1)} & \text{when} \quad \Psi \leq -H \\ \text{change to OFF (0)} & \text{when} \quad \Psi \geq +H \end{cases} \tag{51}$$

The switching circuit designed to implement the hysteresis band, which also imposes the control law given in (51), must be supplied with single-ended voltage to avoid the need for dual-polarity voltage sources. Therefore, the switching function must be raised on a positive offset to avoid negative values. On the other hand, the implementation of the hysteresis band is performed using a hysteresis comparator based on an operational amplifier. Figure 9 shows the proposed switching circuit implementation, which includes three main parts: first, a zener network is used to generate the positive offset, which raises Ψ on a V_z offset voltage (V_z is the zener voltage); second, a positive adder to sum both Ψ and V_z; third, the hysteresis comparator reported in [26].

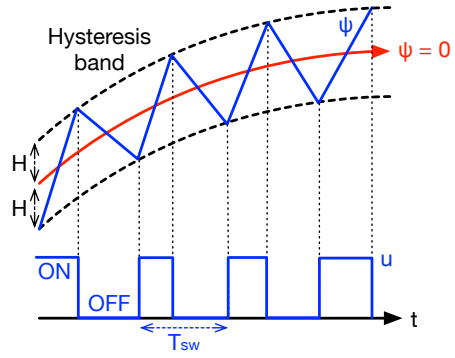

Figure 8. Hysteresis band to limit the switching frequency.

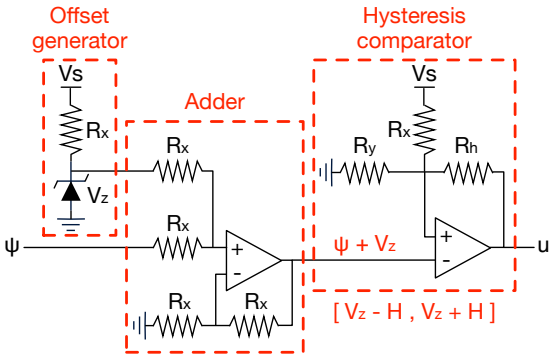

Figure 9. Switching circuit implementing the control law (51).

Defining the hysteresis width as H, the hysteresis limits must be $[V_z - H, V_z + H]$. Then, the equations for designing the hysteresis comparator, given in [26], are applied to calculate the R_h and R_y resistances in terms of R_x resistance as given in (52), where V_s is the single-ended voltage supply.

$$R_h = \frac{V_z - H}{2 \cdot H} \cdot R_x \quad \wedge \quad R_y = \frac{V_z - H}{V_s - V_z - H} \cdot R_x \tag{52}$$

The resistances of both the offset generator and adder are considered equal to R_x for simplicity. Such R_x resistance is selected depending on the characteristics of the operational amplifiers used in the implementation, typically between 10 kΩ and 500 kΩ. The zener voltage V_z is selected as $V_s/2$ to provide the same positive and negative dynamic range to Ψ. Finally, the calculation of the hysteresis band H depends on the maximum switching frequency supported by the MOSFETs, which is analyzed in the following subsection.

3.5. Switching Frequency and H Calculation

The switching frequency F_{sw} imposed by the SMC is calculated from the ripples of the signals into the switching function. The stable operation of the SMC switching function (41) guarantees that $\Psi = 0$, which imposes the following closed-loop dynamics:

$$i_1 \cdot (1 - d) = i_2 \cdot d \quad \wedge \quad (i_1 + i_2) - i_{pv} = i_r \tag{53}$$

Therefore, the average values of both the first and second components in (41) are equal to zero. However, the current ripples of i_1 and i_2 are in phase, as reported in (23) and (24); thus, their magnitudes are additive: $i_1 + i_2 - i_{pv} - i_r = \delta i_1 + \delta i_2$ and $i_1 \cdot (1 - d) - i_2 \cdot d = \delta i_1 \cdot (1 - d) - \delta i_2 \cdot d$. Finally, the ripple of the switching function, which corresponds to the hysteresis band H, is calculated from (41), (23), and (24) as follows:

$$H = \frac{v_{pv} \cdot d}{2 \cdot F_{sw}} \cdot \left[\frac{2 - d}{L_1} + \frac{1 - d}{L_2} \right] \tag{54}$$

It must be pointed out that H must be calculated for the maximum practical value of the switching frequency supported by the MOSFETs used in the NEC boost converter.

4. Design of the PV Voltage Dynamics

The design of the PV voltage dynamics is important for two main reasons:

- Perturbations on the solar irradiance must be mitigated to avoid a large charge on the PV voltage.
- Design equations for the P&O algorithm are provided in terms of the PV voltage [27,28].

The complete control structure of the PV system is summarized in Figure 10, where a voltage controller is introduced between the SMC and the P&O algorithm to define the PV voltage dynamics. Such a voltage controller is based on a PI structure, which imposes the reference of the SMC to ensure the tracking of the voltage reference v_r defined by the P&O.

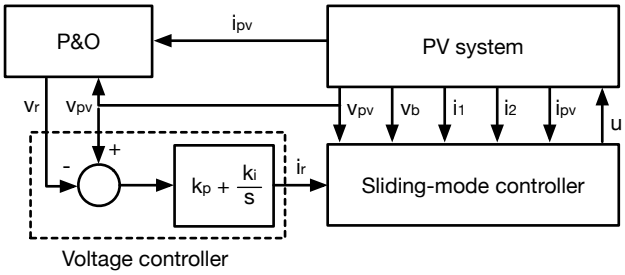

Figure 10. Complete control structure.

The stable operation of the SMC, discussed in (53), defines the control signal u; thus, the averaged model (14)–(17) can be rewritten considering the SMC closed-loop dynamics:

$$\frac{dv_{cb}}{dt} = \frac{i_1 \cdot (1-d) - i_2 \cdot u}{C_{cb}} = 0 \quad \Rightarrow \quad \text{Stable } v_{cb} \text{ voltage} \tag{55}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - (i_1 + i_2)}{C_{pv}} = \frac{-i_r}{C_{pv}} \tag{56}$$

Then, applying the Laplace transformation to the closed-loop relation in (56) leads to the following transfer function:

$$\frac{v_{pv}}{i_r} = \frac{-1}{C_{pv} \cdot s} \tag{57}$$

From the control structure of Figure 10, the Laplace relation between the voltage reference v_r, the PV voltage v_{pv}, and the current reference i_r is observed. Then, the closed-loop transfer function between the PV voltage and reference value, considering the effect of both the voltage controller and SMC, is the following one:

$$\frac{v_{pv}}{v_r} = \frac{k_p \cdot s + k_i}{C_{pv} \cdot s^2 + k_p \cdot s + k_i} \tag{58}$$

4.1. Parameters Design

The PV voltage behavior is designed considering real and equal poles $(s-P)^2$ for the closed-loop transfer function (58). The magnitude P of the poles is given in (59), which requires the value of k_i given in (60) to ensure that both poles are real and equal.

$$P = \frac{k_p}{2 \cdot C_{pv}} \tag{59}$$

$$k_i = \frac{k_p^2}{4 \cdot C_{pv}} \tag{60}$$

The largest deviation in the PV voltage (58) occurs when the voltage reference v_r exhibits step changes, which is the most common waveform of the P&O reference. Equation (61) formalizes such a step change in the Laplace domain, where Δv_{po} is the perturbation magnitude imposed on the P&O algorithm.

$$v_r = \frac{\Delta v_{po}}{s} \tag{61}$$

Then, replacing the previous v_r waveform into the transfer function (58), considering the k_i value given in (60), and applying the inverse Laplace transformation, leads to the following time-domain waveform of v_{pv}:

$$v_{pv} = \Delta v_{po} \cdot \left[1 + (P \cdot t - 1) \cdot e^{-P \cdot t}\right] \tag{62}$$

The P&O algorithm design requires two parameters [27]: the first one is the perturbation magnitude Δv_{po}, already used to obtain expression (62); the second one is the perturbation period T_a, which defines the interval between perturbations. Femia et al. demonstrated in [27,28] that a stable operation of the P&O requires a T_a longer than the settling time t_s of the PV voltage (i.e., $t_s < T_a$). Moreover, Femia also demonstrated that such a settling time changes with the irradiance value imposed by the environmental conditions. Therefore, the voltage controller must be designed to ensure such a stability requirement.

The settling time is calculated when the PV voltage enters an acceptable band $[1 - \epsilon, 1 + \epsilon]\%$ around the final value, where the most commonly adopted band is $\epsilon = 2\%$. Then, the settling time is calculated when $v_{pv} = \Delta v_{po} \cdot (1 + \epsilon)$, which is solved using expression (62) as given in (63), where $W(\cdot)$ is the Lambert-W function.

$$t_s = \frac{1 - W\left(-\epsilon \cdot e^1\right)}{P} \tag{63}$$

Substituting the value of P, given in (59), into the previous expression enables to calculate the k_p value required to impose the desired settling time t_s:

$$k_p = 2 \cdot C_{pv} \cdot \frac{1 - W\left(-\epsilon \cdot e^1\right)}{t_s} \tag{64}$$

4.2. Implementation of the Complete Control Structure

An efficient implementation of the complete control structure requires reformulating the switching function (41) to reduce the mathematical operations. Therefore, the mathematical expression of the switching function is condensed as $\Psi = i_1 \cdot (2 - d) + i_2 \cdot (1 - d) - i_{pv} - i_r$. Moreover, from (22), it is calculated that $(2 - d) = 1 + \frac{v_{pv}}{v_b}$ and $(1 - d) = \frac{v_{pv}}{v_b}$. Using those simplifications, the block diagram of the complete control structure is presented in Figure 11, where the switching circuit was previously designed in Figure 9. The block diagram shows the variables needed to be measured: the PV voltage is used in the calculation of the P&O algorithm, voltage controller, and SMC; the PV current is used in the calculation of both the P&O algorithm and SMC; while the output voltage v_b and the inductor currents (i_1 and i_2) are used for the SMC calculation.

Such an implementation of Figure 11 can be performed using a digital embedded processor, such as the TMS320F28335 from Texas Instruments [29], which enables to implement the complete block diagram into a single device. However, the calculation of Ψ can also be performed using analog hardware: the additions, subtractions, integrations, and static gains (k_p and k_i) can be implemented with operational amplifiers, while the static value can be set with a Zener diode as depicted in the switching circuit of Figure 9. The multiplication and division operations can be implemented with analog multipliers and dividers, which are available as integrated circuits such as the AD533 [30], RC4200 [31], and HA-2557 [32]. It is important to note that the P&O algorithm requires a digital device;

thus, calculating Ψ inside the digital processor is a much more convenient solution since no additional hardware is required.

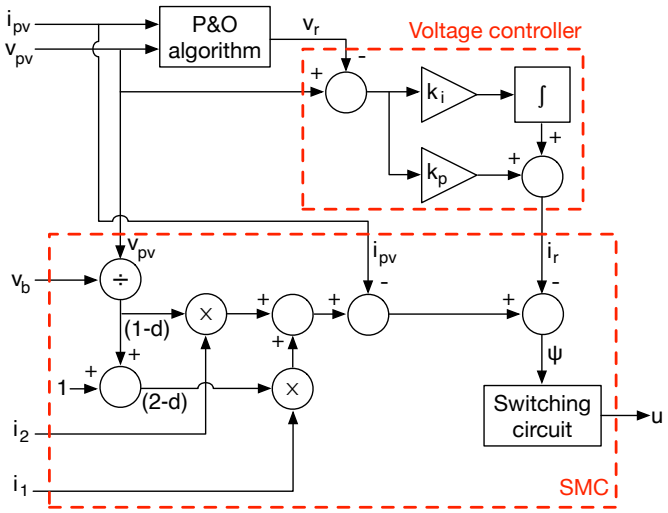

Figure 11. Implementation of the complete control structure.

5. Design Procedure and Application Example

The PV system is designed depending on the operation conditions required by the PV panel and grid-connected inverter (or micro/nanogrid). For this application example, a BP585 PV panel is selected to be interfaced with a $v_b = 48$ V DC-link, which is common for low-voltage nanogrids and some commercial inverters (e.g., ATO-GTI-300 inverter), but any other panel and bus voltage can be considered depending on the application. The datasheet parameters of the BP585 PV panel are reported in Table 1 [33].

Table 1. Datasheet parameters of the BP585 PV panel [33].

Parameter	Value
Maximum Power (P_{mpp})	85.0 W
Voltage at P_{mpp} (V_{mpp})	18.0 V
Current at P_{mpp} (I_{mpp})	4.72 A
Short-circuit current (I_{sc})	5.0 A
Open-circuit voltage (V_{oc})	22.1 V

The first step to design the PV system is to define the desired current and voltage ripples. Taking into account that the P&O algorithm could provide a precision higher than 99%, as demonstrated in the works reported in [27,28], the PV voltage ripple must be lower than 1% of the optimal operation voltage, which in Table 1 is V_{mpp} = 18 V. Therefore, this example considers the desired peak-to-peak ripple of the PV voltage equal to 0.1% of V_{mpp}, i.e., $\delta v_{pv} \leq 9$ mV.

The main advantage of the NEC boost converter, in comparison with the classical boost converter, is the capability to provide a continuous current to the output DC bus. This is possible since the current provided by the NEC boost converter is i_2, which is continuous when the ripple δi_2 (24) of that current is smaller than the average value $\langle i_2 \rangle$. Therefore, L_2 will be designed to provide a continuous current for at least 75% of the irradiance space: Figure 12 shows the electrical characteristics of the PV panel for the maximum irradiance possible (1000 W/m^2), and for the 75% (750 W/m^2), 50% (500 W/m^2), and 25% (250 W/m^2) of such an irradiance space. Thus, L_2 must be designed to provide $\delta i_2 \leq \langle i_2 \rangle$ for irradiances $S \geq 250$ W/m^2 (green zone of Figure 12). For irradiances $S < 250$ W/m^2, the L_2 current will be discontinuous (red zone of Figure 12), but the power provided to the DC-link will be low; thus, the high-frequency current components will also have a low

impact on the DC-link. Finally, L_2 could be designed to impose a continuous current for a larger irradiance space depending on the requirements of the second stage.

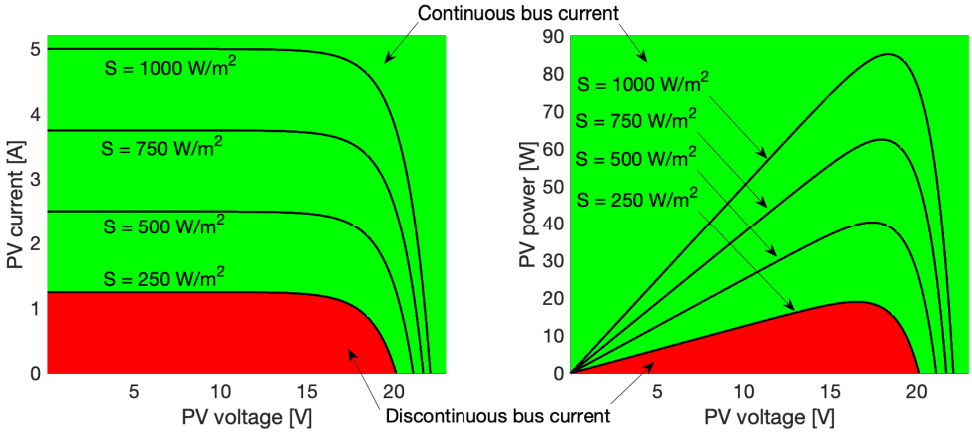

Figure 12. Electrical characteristics of the PV panel.

The MPP conditions of the PV panel under an irradiance of 250 W/m^2 are $I_{mpp@250} = 1.15$ A and $V_{mpp@250} = 16.5$ V, which produce a duty cycle $d = 0.656$ for the NEC boost converter (22); those values assume a temperature of 25 °C (i.e., the STC temperature considered in the datasheet). For different temperature conditions, the MPP current and voltage can be extracted from experimental measurements or estimated using a model parameterized at the desired temperature. Then, using expressions (18) and (21) it is calculated the average value of i_2 as $\langle i_2 \rangle = I_{mpp@250}/(1 + d/(1 - d)) = 0.39$ A. Therefore, the current ripple on L_2 must be $\delta i_2 \leq 0.39$ A when $S = 250$ W/m^2.

The electrical scheme of Figure 3 shows that the ripple of the PV current is shared between i_1 and i_2 currents; hence, $L_1 = L_2$ is selected to ensure a balanced sharing of the current ripple, which is confirmed by expressions (23) and (24). On the other hand, the voltage of the internal capacitor C_{cb} affects the derivative of both i_1 and i_2, as reported in (9) and (10); hence, C_{cb} must be designed to have a small voltage ripple δv_{cb}. Therefore, δv_{cb} is selected as 10% of the steady-state value of v_{cb}, which, according to expression (19), is equal to 48 V. In addition, the switching frequency of the NEC boost converter is selected to be below 100 kHz, which ensures the correct operation of commercial MOSFETs as observed in the implementation of the boost converter reported in [25]. Finally, Table 2 summarizes the design characteristics for the NEC boost converter for this example.

Table 2. Design characteristics for the NEC boost converter.

Parameter	Value
L_2 current ripple	$\delta i_2 \leq 0.39$ A at $S = 250$ W/m^2
L_1 inductor	$L_1 = L_2$
C_{cb} voltage ripple	$\delta v_{cb} \leq 4.8$ V
PV voltage ripple	$\delta v_{pv} \leq 9$ mV
Switching frequency	$F_{sw} \leq 100$ kHz

Applying Equation (24) leads to a minimum L_2 inductance of 147 µH; so, the commercial values $L_1 = L_2 = 150$ µH are selected. Similarly, applying Equation (25) leads to a minimum C_{cb} capacitance of 1.13 µF, selecting a commercial value $C_{cb} = 1.2$ µF for this application. The C_{pv} capacitance is calculated from Equation (26) using the values of $\delta i_1 = \delta i_2$, which results in a minimum capacitance of 108.33 µF; thus, the commercial value $C_{pv} = 110$ µF is adopted.

The parameters of the P&O algorithm are calculated following the procedure proposed by Femia et al. in [34], obtaining a perturbation period $T_a = 500$ µs and a perturbation magnitude $\Delta v_{po} = 200$ mV. Since Femia also demonstrated that the settling time of the PV

voltage must be shorter than T_a to ensure the P&O stability, such a settling time is defined as $t_s = 400\ \mu s < T_a$. Concerning the SMC, Equation (54) is used to calculate the hysteresis width needed to limit the switching frequency under 100 kHz, obtaining $H = 0.667$ A. Then, the voltage controller parameters are calculated from Equations (60) and (64) to ensure the desired t_s value, obtaining $k_p = 2.96$ A/V and $k_i = 19.98$ kA/V.

It is important to remark that the global stability of the SMC is ensured when the dynamic restrictions (47) and (48) are fulfilled. Those limits depend on the derivative of the PV current, which can be analyzed using the ideal single diode model, whose parameters are calculated following the procedure reported in [35]: $i_{pv} = i_{sc} - A \cdot e^{B \cdot v_{pv}}$, where $A = 896.8\ nA$, $B = 0.7029\ \mathrm{V}^{-1}$, and the short-circuit current is considered proportional to the irradiance condition S as $i_{sc} = (5/1000) \cdot S$. Then, the PV current derivative is $\frac{di_{pv}}{dt} = \frac{di_{sc}}{dt} - A \cdot B \cdot e^{B \cdot v_{pv}}$, where $\frac{di_{sc}}{dt}$ is proportional to the derivative of the irradiance $\frac{dS}{dt}$. In order to test the proposed solution under strong perturbations, a very fast change on the irradiance condition $\frac{di_{sc}}{dt} = 1000\ (\mathrm{W/m^2})/\mathrm{ms}$ is considered, which corresponds to a change of one sun in a single millisecond, i.e., from fully irradiated to completely shaded in one millisecond. Evaluating the limits given in (47) and (48) results in $-0.35\ \mathrm{A}/\mu\mathrm{s} < \frac{di_r}{dt} < 0.21\ \mathrm{A}/\mu\mathrm{s}$, but with the aim of imposing a single dynamic limit, the most restrictive condition is selected as $\left|\frac{di_r}{dt}\right| < 0.21\ \mathrm{A}/\mu\mathrm{s}$. The current reference i_r is provided by the voltage controller as $i_r = k_p \cdot (v_{pv} - v_r) + k_i \cdot \int (v_{pv} - v_r)\ dt$; thus, the dynamic limitation must be described in terms of the voltage reference v_r. Deriving the previous expression for i_r, and replacing $v_{pv} - v_r = \Delta v_{po}$ (change on the reference imposed by the P&O) and $i_{pv} - (i_1 + i_2) = 2 \cdot \delta i_2$ (sum of the current ripples in i_1 and i_2), leads to the dynamic restrictions on the voltage reference to ensure the stability of the SMC as follows:

$$\frac{dv_r}{dt} = \frac{2 \cdot \delta i_2}{C_{pv}} - \frac{1}{k_p} \cdot \left(\frac{di_r}{dt} - k_i \cdot \Delta v_{po} \right) \tag{65}$$

Evaluating the previous expression results in the dynamic restriction $\left|\frac{dv_r}{dt}\right| < 0.061\ \mathrm{V}/\mu\mathrm{s}$, which must be imposed into the reference generated by the P&O algorithm. Such a limitation can be implemented in analog form using operational amplifiers, e.g., using the circuit reported in [36], or by embedding it into the digital processor used to implement the P&O algorithm. This application uses the second option since the digital processor is already needed to execute the P&O algorithm, thus avoiding the use of additional hardware. Such a digital limitation is implemented using expression (66), which generates a ramp with slope $\max\left(\left|\frac{dv_r}{dt}\right|\right)$ to impose the desired perturbation magnitude Δv_{po}; this expression accounts for both positive and negative perturbations.

$$v_{r(k)} = v_{r(k-1)} + \Delta v_{po} \quad \Rightarrow \quad \Delta v_{po} = \pm \max\left(\left|\frac{dv_r}{dt}\right|\right) \cdot t \quad , \quad \forall\ t \in \left[0, \frac{\Delta v_{po}}{\max\left(\left|\frac{dv_r}{dt}\right|\right)}\right] \tag{66}$$

Finally, the designed parameters for both the NEC boost converter and SMC are reported in Table 3, and the design process of those parameters is summarized in the flowchart of Figure 13: the PV panel used in the installation and the maximum switching frequency supported by the MOSFETs must be defined; then, the PV model parameters are calculated using the procedure reported in [35]. Using the previous information, the values for the inductors of the NEC boost converter are calculated using expressions (18)–(24). The next step is to calculate the C_{cb} capacitor using expression (25), and the input capacitor C_{pv} is designed from Equation (26). The voltage and current that must be supported by both semiconductors are calculated from (27) to (30), which are needed to select the MOSFET and diode. The parameters of the P&O algorithm are calculated using the procedure reported in [34], and the settling time t_s of the PV voltage must be defined to ensure the P&O stability ($t_s < T_a$). Using expression (54), the hysteresis width H of the SMC is calculated, and the

voltage controller parameters k_p and k_i are calculated using expressions (60) and (64). The control system design is finalized with the calculation of the dynamic limits for the voltage reference using Equations (47), (48), and (65), which is implemented using the difference equation given in (66).

Table 3. Designed parameters for the NEC boost converter and SMC.

Parameter	Value
v_b	48 V
L_1	150 µH
L_2	150 µH
C_{cb}	1.2 µF
C_{pv}	110 µF
t_s	400 µs
H	0.667 A
k_p	2.96 A/V
k_i	19.98 kA/V
$\max\left(\left\|\frac{dv_r}{dt}\right\|\right)$	0.061 V/µs

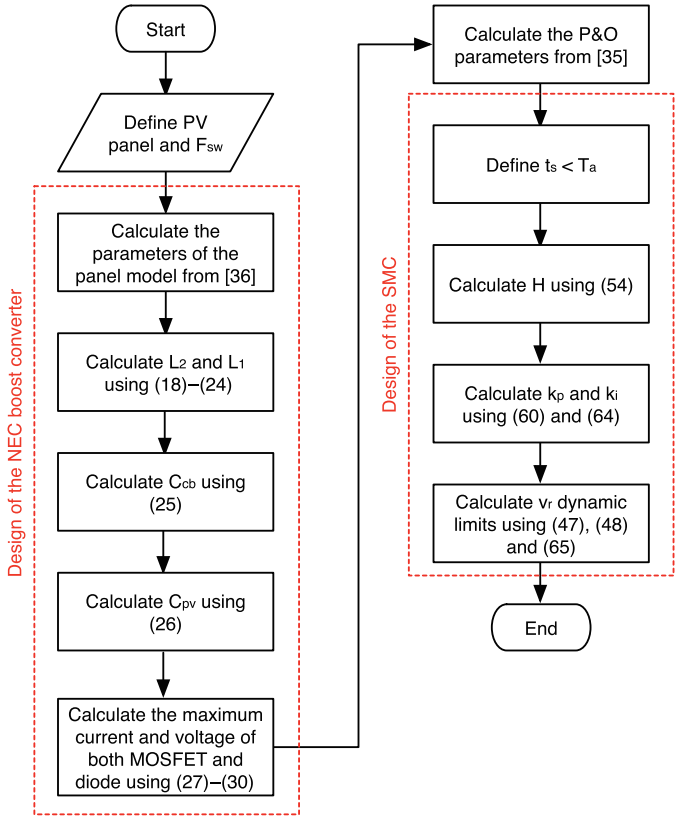

Figure 13. Design process for both the NEC boost converter and SMC.

6. Validation Using Circuital Simulations

The validation of the proposed PV system is performed using realistic and detailed simulations in the commercial power electronics simulator PSIM [20], which is used by several industries due to the capability to simulate the non-linear behavior of the MOSFET and diode, parasitic effects, and even emulate microprocessors using a C-code interface.

The detailed circuital simulation is carried out using the circuital description of the PV system given in Figure 2. The controller block of such a figure is formed by the complete structure depicted in Figure 11, which uses the switching circuit of Figure 9 to generate the control signal u of the NEC boost converter. Finally, the circuital simulation is configured

using the parameters for both the NEC boost converter and SMC reported in Table 3, while the switching circuit is supplied with a $V_s = 5$ V power source and implemented using a Zener diode with $V_z = 2.5$ V, resulting in $R_x = R_y = 20$ kΩ and $R_h = 27.5$ kΩ. Figure 14 shows the PSIM implementation of the PV system based on the NEC boost converter, including the SMC: in this circuit, the implementation of both the voltage controller and the calculation of the switching function Ψ are performed in an emulated microprocessor, which acquires the required signals using Analog-to-Digital converters (ADC) and delivers the output Ψ using a Digital-to-Analog converter (DAC). Appendix A reports the C code developed for the microprocessor, which can be used to implement those processes in any real device programmable in C language.

The main advantage of the NEC boost converter concerns the reduced harmonic content introduced to the output DC bus in comparison with the classical boost topology. Such a condition is tested by comparing the performance of the proposed NEC solution with an equivalent PV system based on a boost converter: to provide a fair comparison, the boost converter is designed to provide the same current and voltage ripple to the PV panel; therefore, the capacitor and inductor of the boost topology are $C_{boost} = 110$ μF and $L_{boost} = 75$ μH, respectively. The design of such a boost inductor is also fair in terms of stored energy, as discussed in Section 2.2: the boost inductor stores almost the same energy as the two inductors of the NEC option. In fact, for a duty cycle of 50%, both L_1 and L_2 support half of the PV current, resulting in a combined stored energy of $\frac{1}{2} \cdot L_1 \cdot (i_{pv} \cdot 0.5)^2 + \frac{1}{2} \cdot L_2 \cdot (i_{pv} \cdot 0.5)^2 = 37.5 \times 10^{-6} \cdot i_{pv}^2$, where $L_1 = L_2 = 150$ μF; the energy stored in the inductor of the boost current is $\frac{1}{2} \cdot L_{boost} \cdot i_{pv}^2 = 37.5 \times 10^{-6} \cdot i_{pv}^2$, which is the same. In the extreme case of the MPP at the highest irradiance (1000 W/m^2), the duty cycle is $d = 61.77\%$, which results in a combined energy of the NEC converter inductors equal to $39.57 \times 10^{-6} \cdot i_{pv}^2$, which is only 5.5% higher than the energy stored in the inductor of the boost converter.

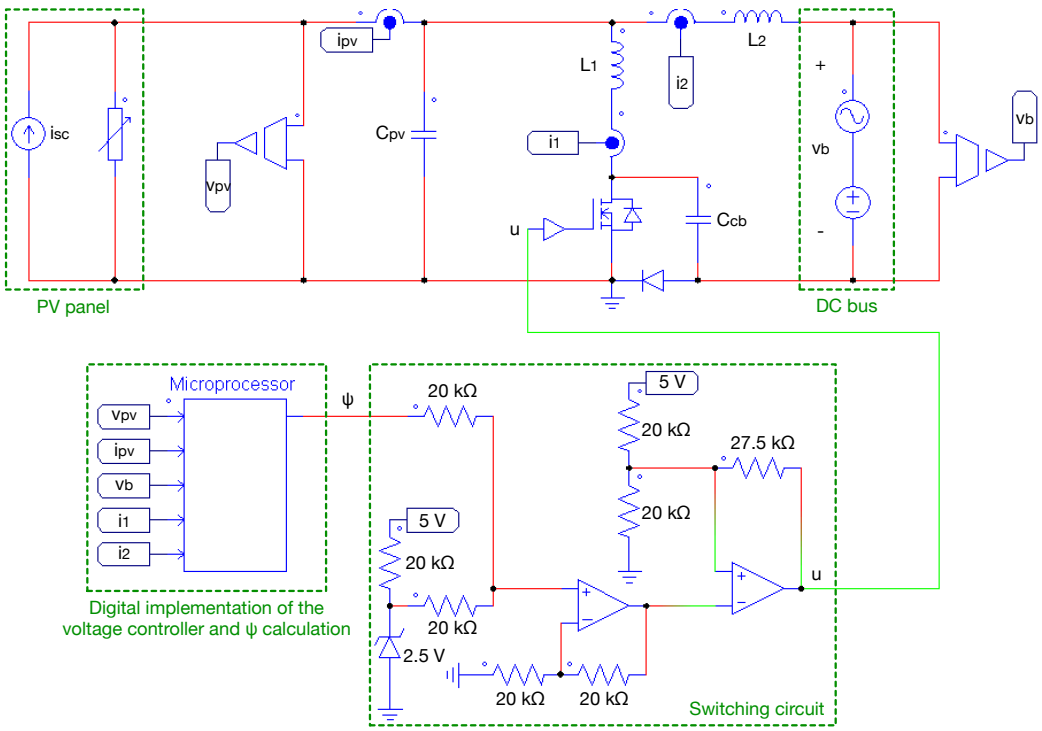

Figure 14. PV system circuit implemented in PSIM.

Figure 15 reports the circuital simulations of the PV systems based on both the NEC and classical boost converters performed in PSIM. The detailed simulations confirm the desired condition for the PV voltage ripple, previously reported in Table 2: the peak voltage ripple is 8.9 mV$<$ 9 mV. Such a value exhibits an error of 2.5% with respect to

the theoretical value calculated from (26), which is mainly caused by the changes on the switching frequency introduced by the SMC. Moreover, the figure confirms that both the NEC and classical boost converters provide the same voltage and current ripples at the PV panel side, verifying the correct design of the classical boost converter and NEC converter input capacitor. The ripple magnitudes of the inductor current reported in this simulation have errors equal to 2.98% with respect to the theoretical values calculated from (23) and (24), which are also caused by the changes on the switching frequency.

The simulation results of Figure 15 confirm the advantage of the NEC topology over the classical boost option: the current delivered to the DC bus by the NEC boost converter (which corresponds to i_2) is continuous, while the current delivered by the classical boost topology (which corresponds to diode current) is discontinuous. In order to provide a numerical comparison, the RMS and DC values of those output currents are calculated: for the NEC boost converter, they are $i_{2,DC} = 1.76$ A and $i_{2,RMS} = 1.78$ A, while for the classical boost converter they are $i_{d,DC} = 1.76$ A and $i_{d,RMS} = 2.90$ A. Then, the AC components of the output currents are $i_{2,AC} = 0.26$ A for the NEC topology and $i_{d,AC} = 2.30$ A for the boost converter, calculated from $i^2_{RMS} = i^2_{DC} + i^2_{AC}$. Therefore, the proposed PV system based on the NEC boost converter introduces nine times less (1/9) undesired current harmonics than a PV system based on the classical boost converter, thus providing a much better power quality to the DC bus or grid-connected inverter. This reduction in the AC current component has a difference of 8% with respect to the values calculated from (39) and (40), which is caused by the change on the duty cycle from $d = 0.5$ (used in the comparison of Section 2.2) to $d = 0.6177$ (set by the MPPT algorithm at 1000 W/m^2).

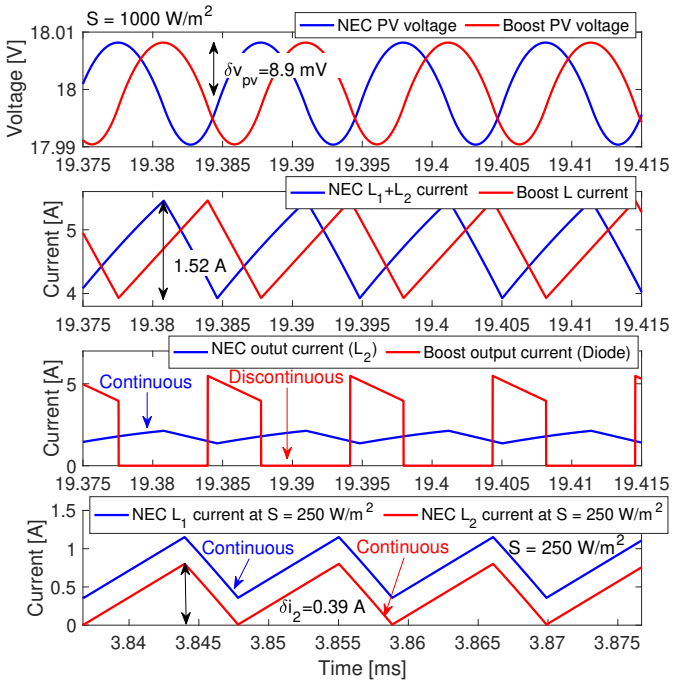

Figure 15. Steady-state operation of the PV system and comparison with the classical boost topology.

The simulation results also report a switching frequency equal to 98.5 kHz at $S = 1000$ W/m^2, which confirms the fulfillment of the practical restriction imposed in Table 2 for the switching frequency ($F_{sw} \leq 100$ kHz). Finally, Table 2 reports that the current of L_2 in the NEC boost converter must fulfill $\delta i_2 \leq 0.39$ A at $S = 250$ W/m^2 to ensure a continuous output current for 75% of the irradiance space (as described in Figure 12). This is verified by Figure 15, which shows (in the bottom waveforms) the behavior of both inductors' currents in the NEC boost converter at $S = 250$ W/m^2, confirming the desired condition. In conclusion, the simulation results reported in Figure 15 confirm the correct design of C_{pv}, L_1, and L_2 for the NEC boost converter.

The stable operation of the proposed PV system is also confirmed by the simulation results of Figure 16, which verify that the ripple condition for v_{cb}, given in Table 2, is fulfilled with an error of 4.5% with respect to the theoretical value calculated from (25), thus confirming the correct design of C_{cb}. In addition, Figure 16 also reports the same steady-state value given in (19) and (20) for v_{cb} and v_{pv}, respectively, and the relation given in (21) for the inductor currents; therefore, the stable operation of the NEC boost converter is confirmed. Finally, this simulation also reports the waveform of the switching function Ψ, thus validating the correctness of the control law defined in Equation (51). In conclusion, the simulation results reported in both Figures 15 and 16 confirm the correct design of both the NEC boost converter and switching circuit.

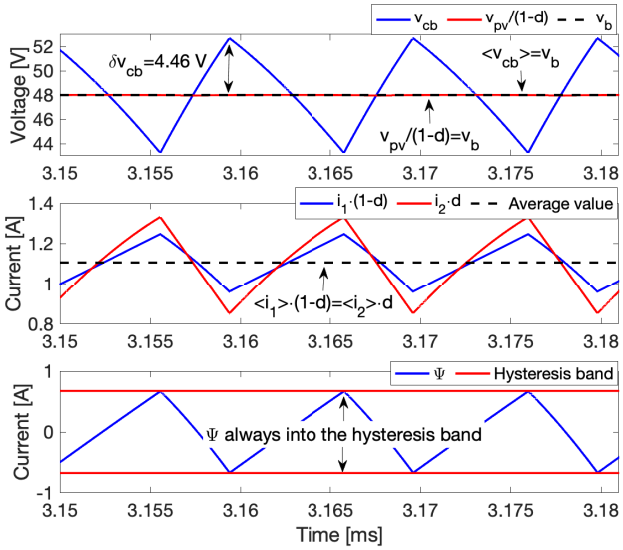

Figure 16. Stable operation of the proposed PV system.

A second simulation was carried out to test both the stability and dynamic performance of the proposed control system. This new simulation introduces a change of Δv_{po} in the voltage reference to test the controller's ability to ensure the desired settling time t_s defined in Table 3. Figure 17 reports the detailed simulation results, where the reference change is imposed at $t = 4.17$ ms with the derivative defined in Table 3 (dashed black waveform v_r), i.e., $\max\left(\left|\frac{dv_r}{dt}\right|\right) = 0.061$ V/µs. This simulation also includes the verification of the theoretical dynamic behavior of the PV voltage reported in Equation (58), which was evaluated using the parameters of Table 3 to obtain the numerical version G_{pv} for this particular example:

$$G_{pv} = \frac{v_{pv}}{v_r} = \frac{2.965 \cdot s + 1.999 \times 10^4}{1.1 \times 10^{-4} \cdot s^2 + 2.965 \cdot s + 1.999 \times 10^4} \tag{67}$$

The simulation results reported in Figure 17, at the top, show the correct prediction of the PV voltage (v_{pv} in blue trace) provided by the theoretical transfer function G_{pv} (red trace), which exhibits an absolute-relative-error (68) of 0.52% that is mainly caused by the switching ripple, thus confirming the correctness of the voltage design dynamics proposed in Section 4. For the calculation of the ARE, v_{sim} corresponds to the voltage obtained in the PSIM circuital simulation, while v_{theo} corresponds to the theoretical value.

$$ARE = 100 \times \frac{\sqrt{\sum_{i=1}^{N} (v_{sim} - v_{theo})^2}}{\sqrt{\sum_{i=1}^{N} (v_{theo})^2}} \ [\%] \tag{68}$$

The waveforms in Figure 17 also confirm the correct tracking on the reference (v_r in dashed black trace) with the desired settling time $t_s = 400$ µs, which validates the accurate voltage control design proposed in Section 4.1. The compensation of such a reference change is introduced, by the voltage controller, into the SMC by means of the current reference i_r, which acts on the switching circuit by means of the switching function Ψ. The simulation results show the waveform of i_r, where the voltage controller compensation can be observed.

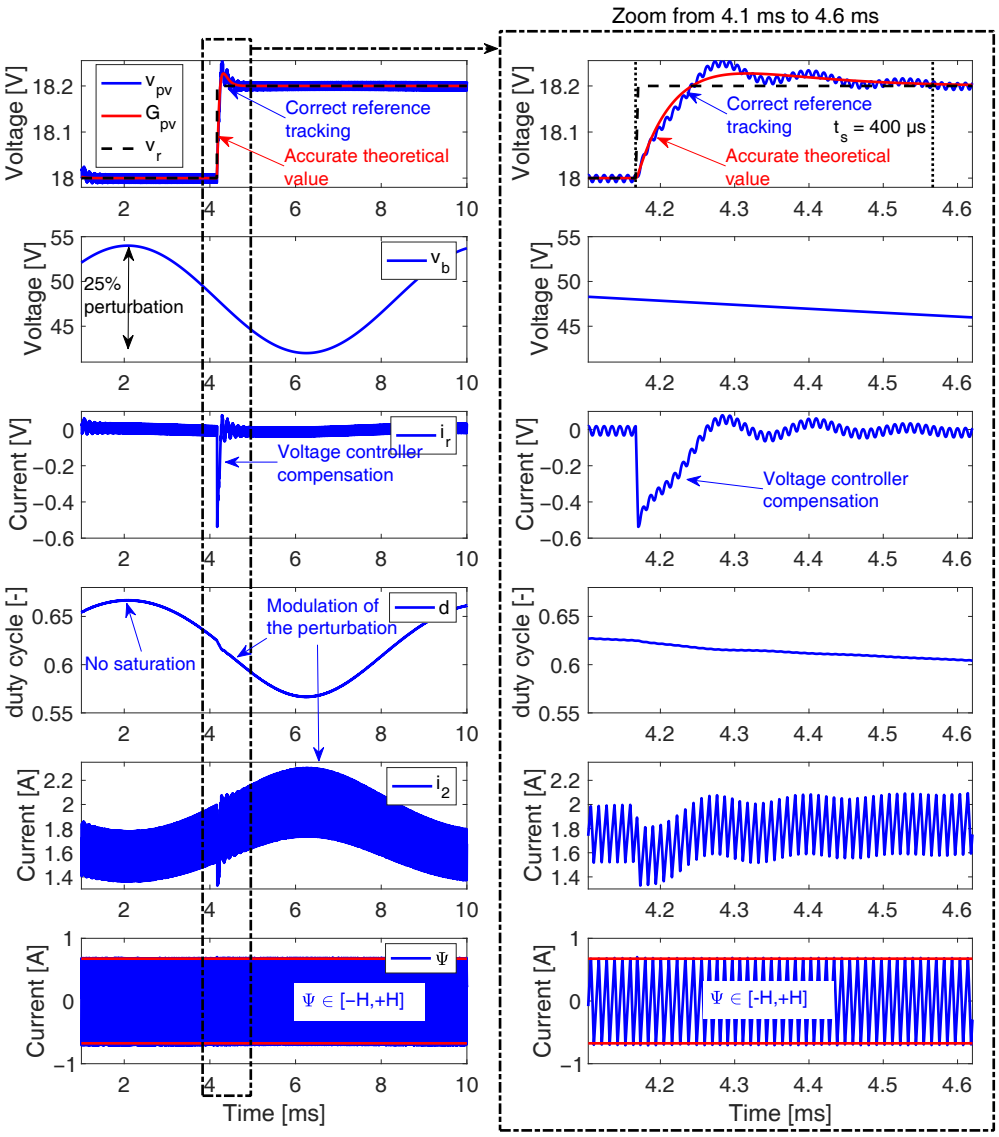

Figure 17. Dynamic performance of the proposed control system.

It is worth noting that this accurate regulation of the PV voltage is performed in presence of a large perturbation in the output voltage v_b (i.e., the DC-link). In this example, the perturbation is equal to a 25% peak-to-peak sinusoidal oscillation at double the grid frequency (120 Hz), which corresponds to the perturbation introduced by a grid-connected inverter with a non-electrolytic DC-link. This perturbation is large in comparison with the DC-link oscillations considered for the validation of other first-stage solutions: Table 4 reports some examples of the peak-to-peak oscillation amplitudes adopted in literature to validate the first stage of microinverters, which are between 1.9 and 500 times smaller than the oscillation adopted in this example, thus requiring a much larger DC-link capacitor.

This comparison provides a measurement of the reduction in the DC-link capacitance requirements obtained with the solution proposed in this paper.

Table 4. Examples of DC-link oscillations reported in literature.

Reference	Peak-to-Peak Oscillation	Compared with the Oscillation Used in the Validation Example
[12]	0.05%	500 times smaller
[13]	2.6%	9.6 times smaller
[11]	13.1%	1.9 times smaller

The simulation results given in Figure 17 also report the duty cycle produced by the SMC, where no saturation occurs ($0 < d < 1$), confirming that the equivalent control condition analyzed in Section 3.3 is fulfilled. In addition, Figure 17 reports the output current i_2 of the NEC boost converter, which is always continuous as expected, hence, providing a much better power quality in comparison with the classical boost converter. Moreover, it is observed that the SMC modulates into i_2 (and d) the perturbation present on v_b, thus avoiding the transmission of such a perturbation into the PV voltage, which ensures stable operation of the PV module even under large output voltage oscillations. Finally, the waveform of the switching function Ψ is always trapped inside the desired hysteresis band $[-H, +H]$ with $H = 0.67$ A; this confirms that both the reachability and transversality conditions analyzed in Sections 3.1 and 3.2 are always fulfilled. In conclusion, the previous results validate the global stability of the SMC in presence of large perturbations, and verify the correct design of the voltage controller to impose the desired behavior to the PV voltage.

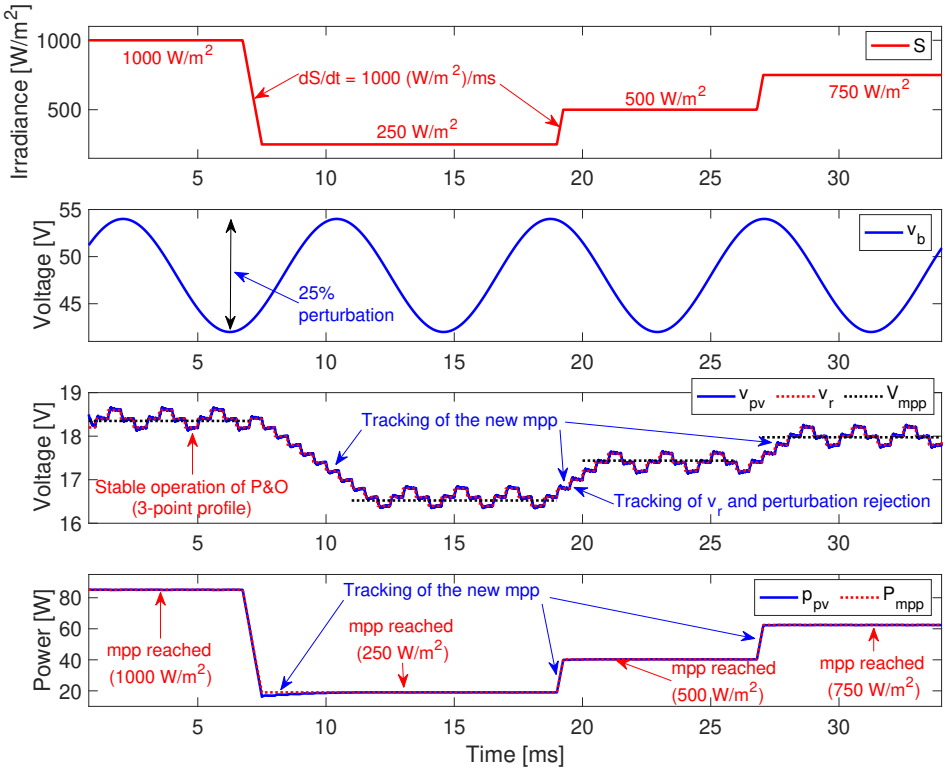

Figure 18. Complete PV system operation under changing irradiance conditions.

A third simulation scenario was designed to evaluate the performance of the complete PV system, including the action of the P&O algorithm. Such a simulation, reported in Figure 18, considers fast changes on the irradiance condition (i.e., high derivatives of 1000 $(W/m^2)/ms$) to test the correct performance of the control system. In particular, the

irradiance starts at the highest value possible (1000 W/m^2), falling to the lowest irradiance considered in this example (250 W/m^2); then, the irradiance changes to 500 W/m^2 and, finally, to 750 W/m^2. The results of this simulation confirm the correct operation of both the P&O algorithm and control system: the PV voltage (v_{pv}) exhibits a 3-point behavior around the MPP voltage (V_{mpp}) for each irradiance condition, thus ensuring that the P&O reference (v_r) reaches the optimal operation condition for every irradiance value as demonstrated in [27,37]. This optimal condition is also confirmed by the power produced by the PV panel (p_{pv}), which always reaches the maximum power possible (P_{mpp}) for every irradiance value. Finally, in the 33.25 ms of this simulation, the complete PV system extracts 99.67% of the maximum energy available, which puts into evidence the correct operation of the system.

Therefore, the simulation scenarios presented in this section validate the following conditions:

- The design process for the NEC boost converter is correct.
- The mathematical analysis of the SMC is correct and practically verifiable.
- The design process for the SMC is correct, ensuring the global stability of the PV system even under the presence of large perturbations.
- The design process for the voltage controller is correct, ensuring the tracking of the reference with the desired settling time.
- The designed PV system, based on the NEC boost converter, ensures the extraction of the maximum PV power and provides a continuous current to the DC-link, resulting much better power quality in comparison with the classical boost converter.

7. Conclusions

This paper proposes a new solution for the first stage of a PV microinverter, which enables the reduction of the DC-link capacitor to non-electrolytic values, thus improving the system reliability. This solution is based on the NEC boost converter and an SMC, providing a precise design process for the complete solution.

The NEC boost converter provides continuous input and output currents, similar to the Cuk converter, but without the voltage inversion, hence simplifying the sensing circuits. Moreover, the proposed PV system imposes lower stress in the internal capacitor and input inductor in comparison with the Cuk converter. The continuous current condition provided by the NEC converter could be also useful to design battery chargers/dischargers, since high-frequency current harmonics affect both the battery health and the DC bus power quality. In addition, the voltage conversion ratio is the same one obtained with a boost converter; hence, the NEC boost topology can be used to replace classical boost converters in existing applications. This could improve the overall efficiency because the RMS current provided by the NEC boost converter is lower than the RMS current provided by the classical boost option, which reduces the ohmic losses on the elements of the second stage. Despite the additional complexity of the NEC boost converter, the paper presents a detailed modeling set formed by the switched model, the averaged model, and the steady-state relations. Those models can be used to design new control strategies for the proposed first PV stage.

The global stability of the proposed SMC was mathematically demonstrated, which enables the first stage to be used in any operation condition including fast-changing irradiance. Moreover, this SMC enables the proposed PV system to be scaled to any power level. However, the dynamic limitation introduced by the reachability conditions must be taken into account in the design; thus, a prior knowledge is needed of the fastest irradiance change to be experimented. This aspect was taken into account in the step-by-step design procedure proposed for the PV system.

The implementation of the proposed control system mixes both analog and digital circuits, which provides flexibility to include additional features such as diagnostic algorithms or more complex MPPT algorithms. In fact, one future improvement is to study the inclusion of MPPT algorithms designed for partially shaded PV systems, which could improve the microinverter's flexibility by enabling the connection of small PV arrays.

In any case, the results obtained in the circuital simulations were satisfactory, since all the theoretical predictions were confirmed with realistic and non-linear simulations. Those results provide confidence to the proposed solution, since the commercial power electronics simulator has been also adopted to validate other microinverters reported in literature. However, the experimental implementation of the proposed first stage will have some challenges that must be addressed in future developments. For example, the resolution of the comparator used in the switching circuit could modify the switching frequency; thus, a safety margin must be introduced into the calculation of the hysteresis width. Another implementation problem to face is the tolerances of the electronics devices; thus, safety margins on the ripple requirements must be also introduced. The largest implementation problem will be the microprocessor interface with the analog circuitry, since the resolution of both the ADC and DAC will introduce errors into the switching function calculation: 10-bit resolution (usually provided in microcontrollers at 5 V) could introduce 4.9 mV errors, which is half of the PV voltage ripple; instead, the suggested microprocessor TMS320F28335 has 12-bit resolution, which only introduces 1.2 mV errors, but at a higher cost in comparison with a traditional microcontroller. Therefore, the correct selection of the microprocessor will have a large impact on the operation of the proposed PV system. Finally, the parasitic losses on the inductors and semiconductors will affect the converter efficiency; hence, a correct balance between low parasitic resistances and element cost must be achieved.

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Data Availability Statement: The data used in this study are reported in the figures and tables of the paper.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

The following nomenclature is used in this manuscript:

C_{cb}	Internal capacitor of the NEC boost converter
C_{pv}	Input capacitor of the converters
d	Duty cycle of the converters
E_1	Energy stored in L_1
E_b	Energy stored in L_b
$E_{L,NEC}$	Energy stored in L_1 and L_2 (both inductors of the NEC boost converter)
F_{sw}	Switching frequency of the converters
H	Width of the hysteresis band used to implement the SMC
i_1	Current of L_1
i_2	Current of L_2
i_{ac}	AC component of the RMS current
i_C	Current of C_{pv}
i_d	Current of the diode in the classical boost converter used for comparison
i_{L_b}	Current of L_b
I_{mpp}	MPP current of the PV module
i_{pv}	Photovoltaic current
i_{RMS}	RMS current

L_1	First inductor of the NEC boost converter
L_2	Second inductor of the NEC boost converter
L_b	Inductor of the classical boost converter used for comparison
p_{pv}	Photovoltaic power
P_{mpp}	MPP power of the PV module
t_s	Settling time of the closed-loop PV voltage
T_{sw}	Switching period of the converters
u	Control signal for the MOSFET of the converters
v_b	Output voltage of the first stage (DC-link voltage)
v_{cb}	Voltage of C_{cb}
v_{pv}	Photovoltaic voltage
V_{mpp}	MPP voltage of the PV module
v_r	Reference voltage provided to the PV voltage controller
δi_1	Switching ripple of i_1
δi_2	Switching ripple of i_2
δv_{cp}	Switching ripple of v_{cb}
δv_{pv}	Switching ripple of v_{pv}
Δv_{po}, T_a	Parameters of the P&O algorithm
ϵ	Band used to calculate the settling time
Ψ	Switching function of the SMC

Abbreviations

The following abbreviations are used in this manuscript:

ARE	Absolute-relative-error
INC	Incremental conductance MPPT algorithm
MPP	Maximum power point
MPPT	Maximum power point tracking
NEC	non-electrolytic-capacitor converter
PI	Proportional–integral
P&O	Perturb and observe MPPT algorithm
PV	Photovoltaic
PSO	Particle swarm optimization
RDAC	Robust direct adaptive controller
RMS	Root-mean-squared
SMC	Sliding-mode controller

Appendix A

This appendix reports the C code developed to implement both the voltage controller and the calculation of the switching function Ψ. The code was used in the microprocessor emulation available in PSIM, but the code can be also used, without major modifications, to implement those processes in any real microprocessor programmable in C language.

```
void SimulationStep( double t, double delt, double *in, double *out, int *pnError, char *
    szErrorMsg, void ** reserved_UserData, int reserved_ThreadIndex, void *
    reserved_AppPtr)
{
 g_nStepCount++;

// Variables to calculate the Perturb and Observe algorithm (P&O)
float Vpv = 0;
float Ipv = 0;
float Ppv = 0;
static float P_old = 0;
float Dvpo = 0.2; // Perturbation magnitude
static float Vr = 18; // Output of the P&O
float Ta = 0.5e-3; // Perturbation period
static float sign = 1; // Perturbation direction of Vpv (1:increase, -1:decrease)
static float t_old = 0;

// Variables to calculate the switching function (Psi)
float Vb;
float i1;
float i2;
```

```
float ir;
float Psi;
float d_1;
float d_2;

// Variables to calculate the voltage controller output (ir)
float e;
static float e_old;
static float ir_old;
float Kp = 1.3479;
float Ki = 9.0847e+03;

// Variables to limit the dynamic response of the P&O reference (dVr/dt)
float ramp_inc = (0.46/1e-6)*delt; // increment with the dynamic limitation
static float ramp = Vr;

// Acquiring the circuit variables using ADC
Vpv = in[0];
Ipv = in[1];
Vb = in[2];
i1 = in[3];
i2 = in[4];

// Calculate the PV power
Ppv = Vpv*Ipv;

// Execute the P&O algorithm each Ta (period)
if( (t-t_old) >= Ta )
{

    // Change the perturbation direction when the power decreases
    if(Ppv <= P_old)
        sign = sign * (-1);

    // Perturbation without dynamic limitation
    Vr = Vr + Dvpo * sign;

    // Avoid reference voltages outside practical values [0, Voc]
    if(Vr < 0)
        Vr = 0;
    if(Vr > 22.1)
        Vr = 22.1;

    P_old = Ppv; // Stored to detect the change on the PV power
    t_old = t; // Stored to detect when period Ta is finished
}

// Ramp to limit dVr/dt
// Increasing ramp with slope max(dVr/dt)
if(ramp < Vr)
{
    ramp = ramp + ramp_inc;
    if(ramp > Vr)
        ramp = Vr;
}
// Decreasing ramp with slope max(dVr/dt)
if(ramp > Vr)
{
    ramp = ramp - ramp_inc;
    if(ramp < Vr)
        ramp = Vr;
}
// The variable ramp corresponds to Vr with the dynamic limitation

// Calculation of the PV voltage controller output (ir)
e = Vpv - ramp; // PV voltage error
ir = ir_old + Kp*e - (Kp - Ki*delt)*e_old; // Difference equation of a PI
e_old = e; // Stored to calculate ir
ir_old = ir; // Stored to calculate ir

// Calculation of the switching function (Psi)
d_1 = (Vpv/Vb); // calculation of (1-d)
d_2 = d_1+1; // calculation of (2-d)
Psi = (d_1*i2) + (d_2*i1)-Ipv-ir; // calculation of Psi

// Delivering Psi to the switching circuit using a DAC
out[0] = Psi;
}
```

Code.c

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